Telkom University

School of Electrical Engineering

(MOS-FET) Metal Oxide Semiconductor Field-Effect Transistors

Microelectronic Circuits - Fifth Edition © Sedra/Smith®

Prodi S1-SK

2017

Why MOSFET ?

Bipolar Junction Transistor Structure

1. 3 Layers
2. Difficult to make, especially in sub micron

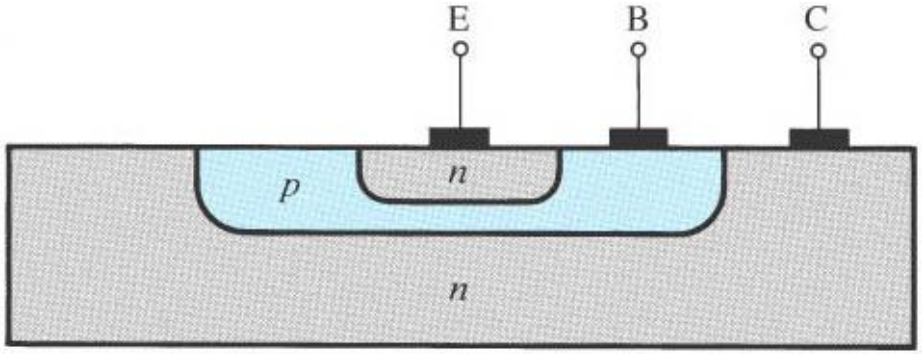
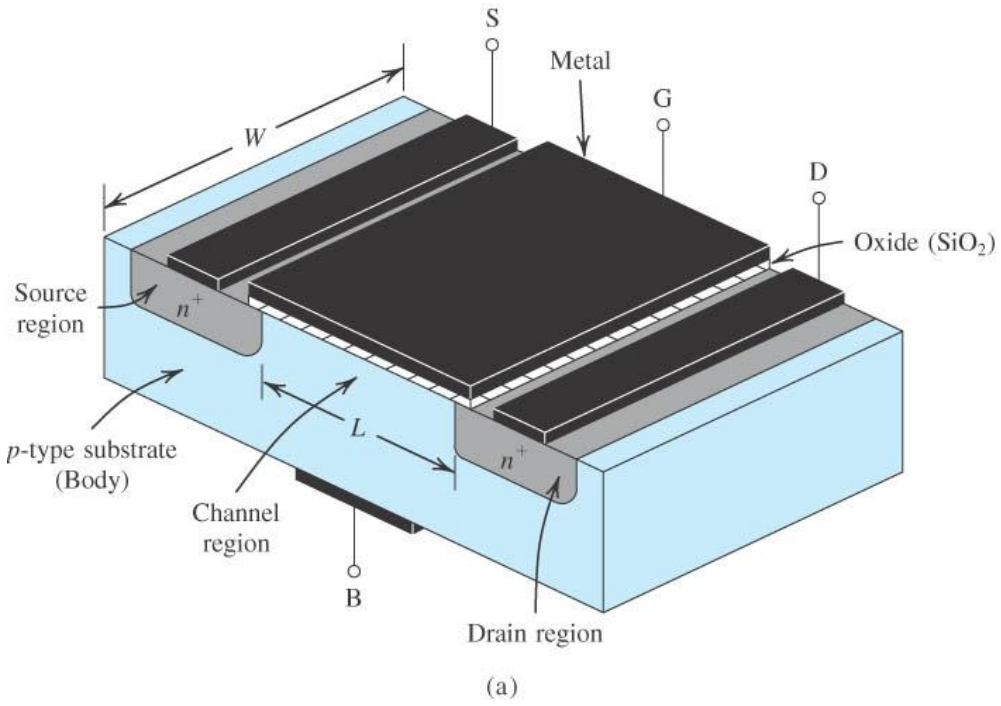


Figure 1. Cross-section of an *npn* BJT.

MOSFET Structure



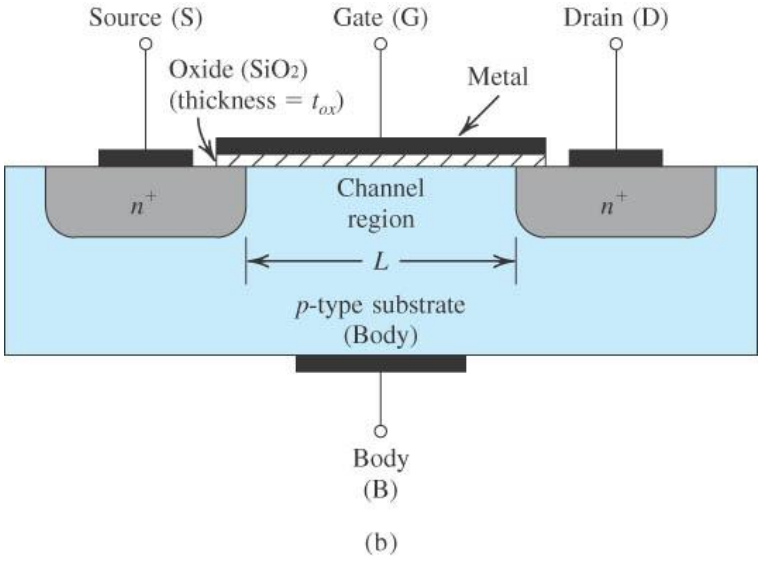


Figure 2. Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross-section. Typically L = 0.1 to 3 μm, W = 0.2 to 100 μm, and the thickness of the oxide layer (t_{ox}) is in the range of 2 to 50 nm.

How MOSFET Works

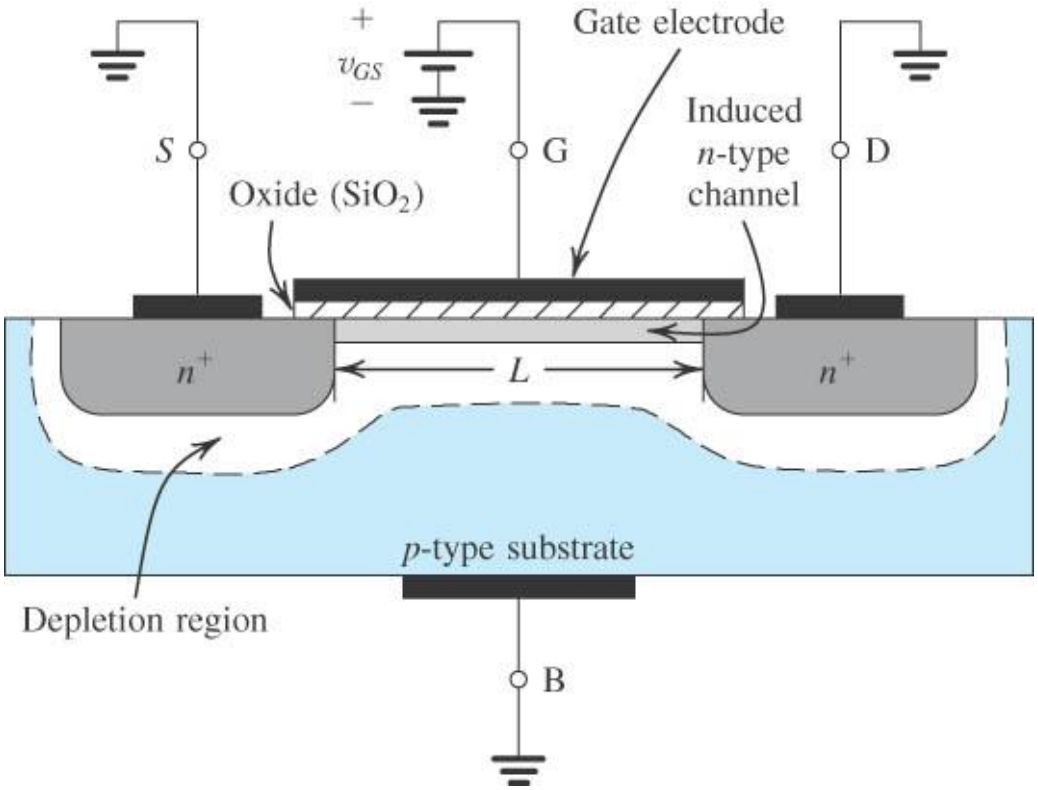
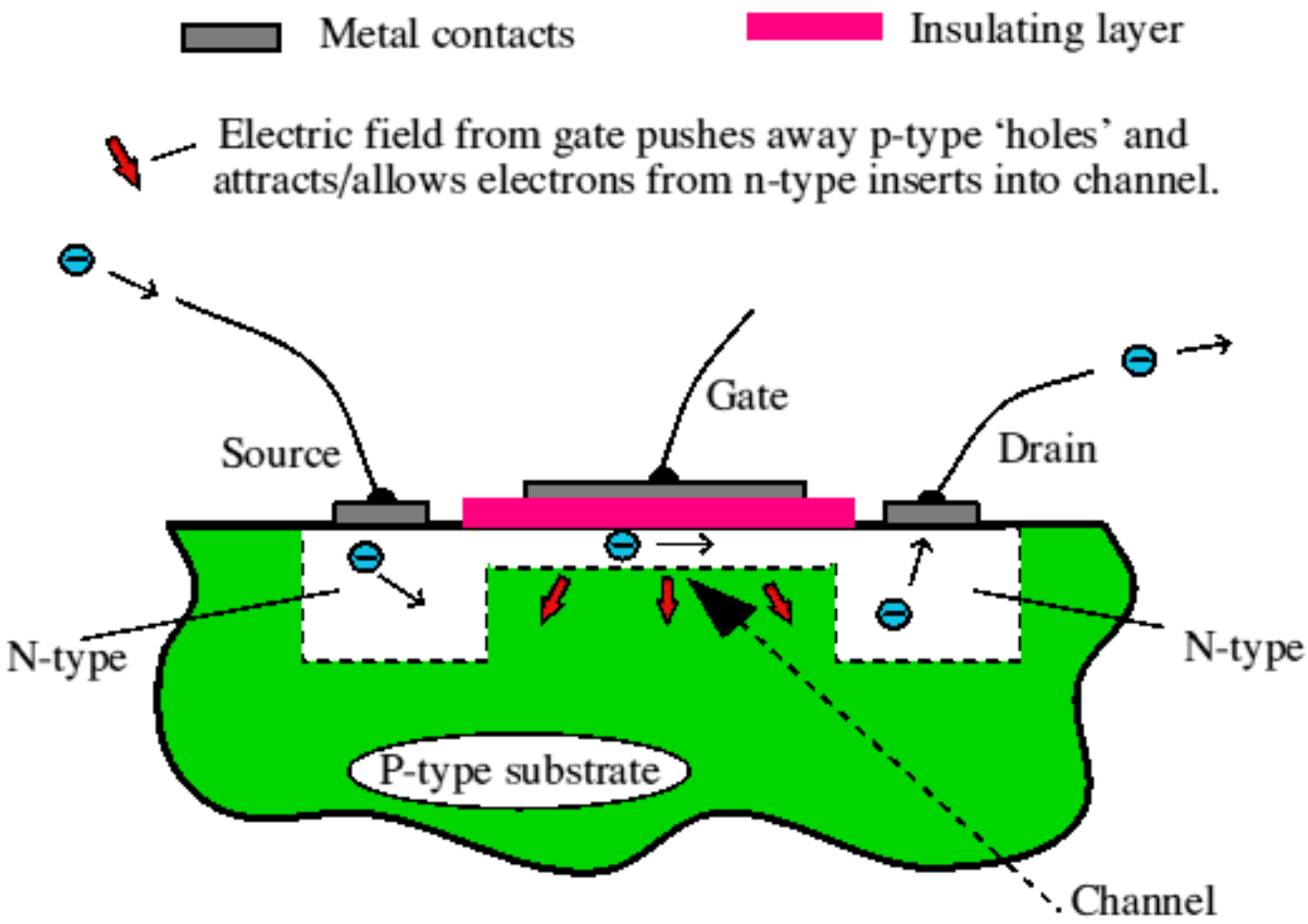


Figure 3. The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

How MOSFET Works



How MOSFET Works

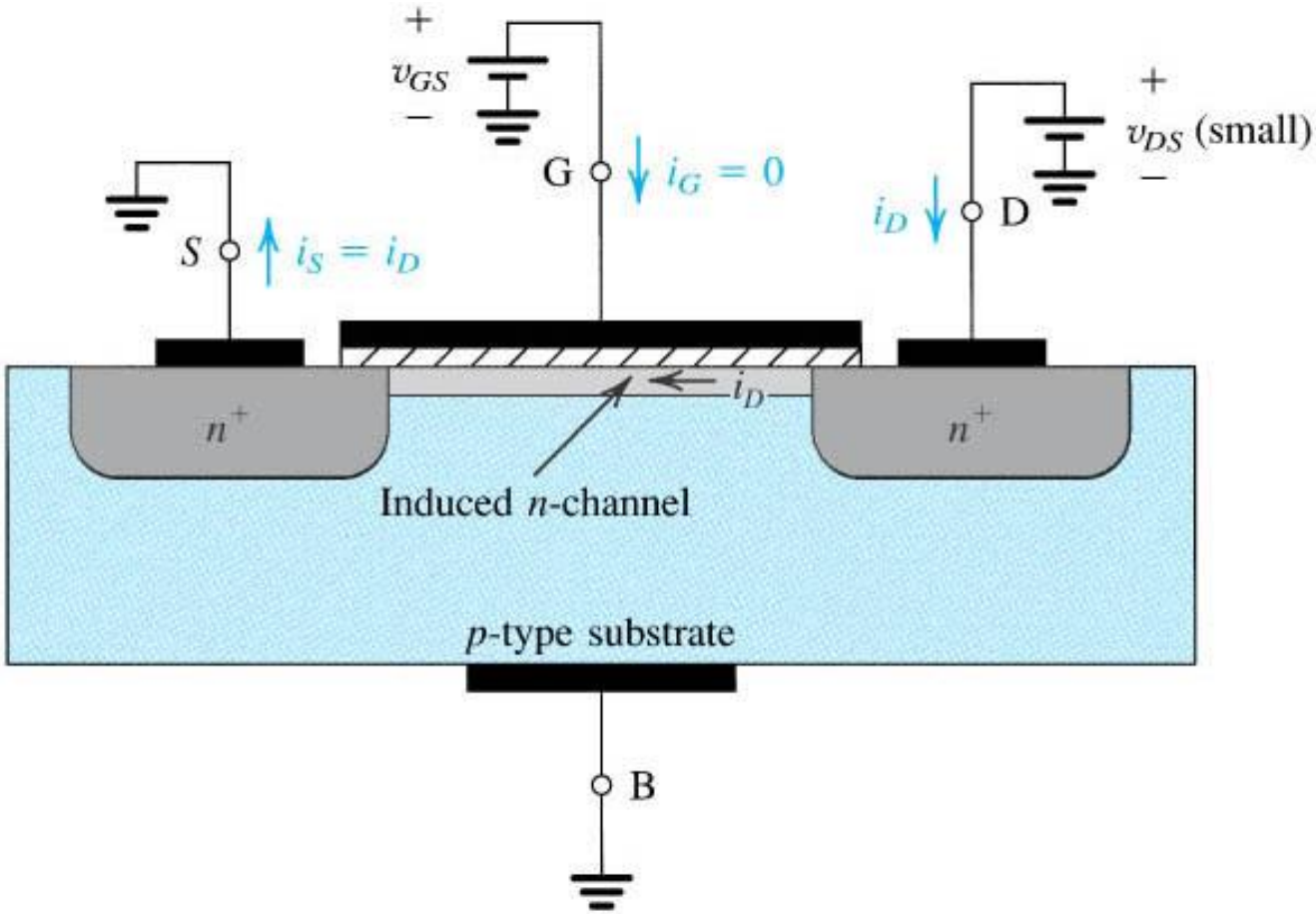


Figure 4. An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)\, v_{DS}$. Note that the depletion region is not shown (for simplicity).

How MOSFET Works

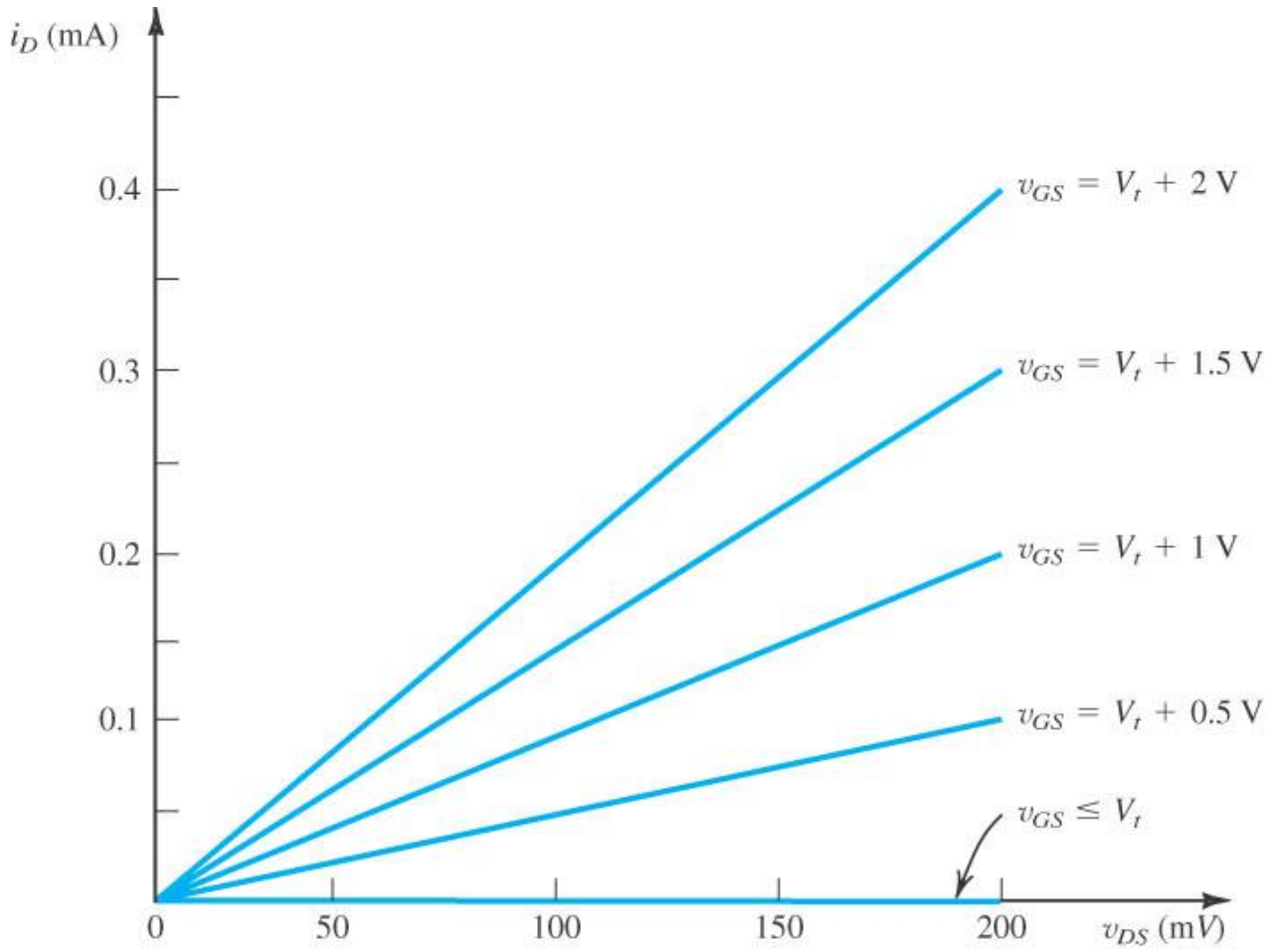


Figure 5. The i_D–v_{DS} characteristics of the MOSFET in Fig. 4.3 when the voltage applied between drain and source, $v_{DS,}$ is kept small. The device operates as a linear resistor whose value is controlled by v_{GS}.

How MOSFET Works

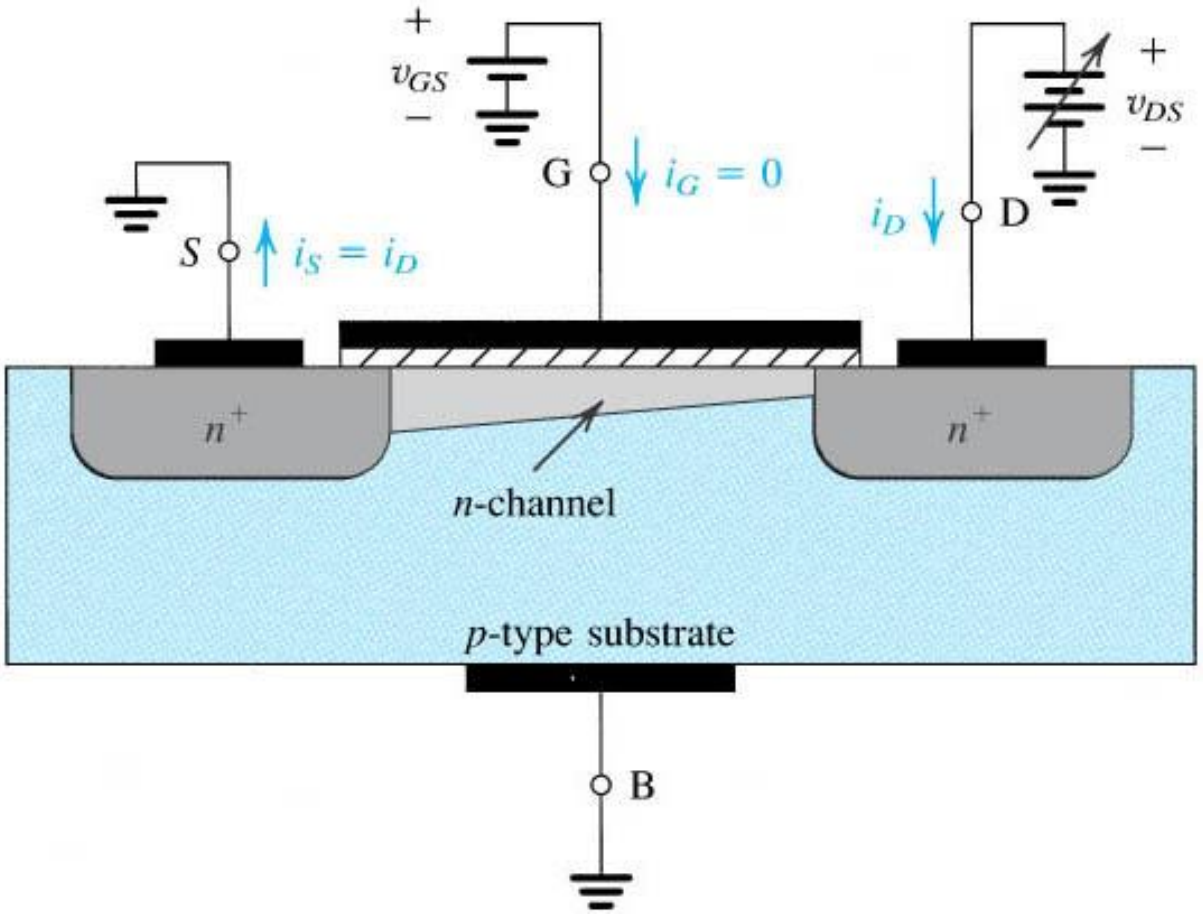


Figure 6. Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t.

How MOSFET Works

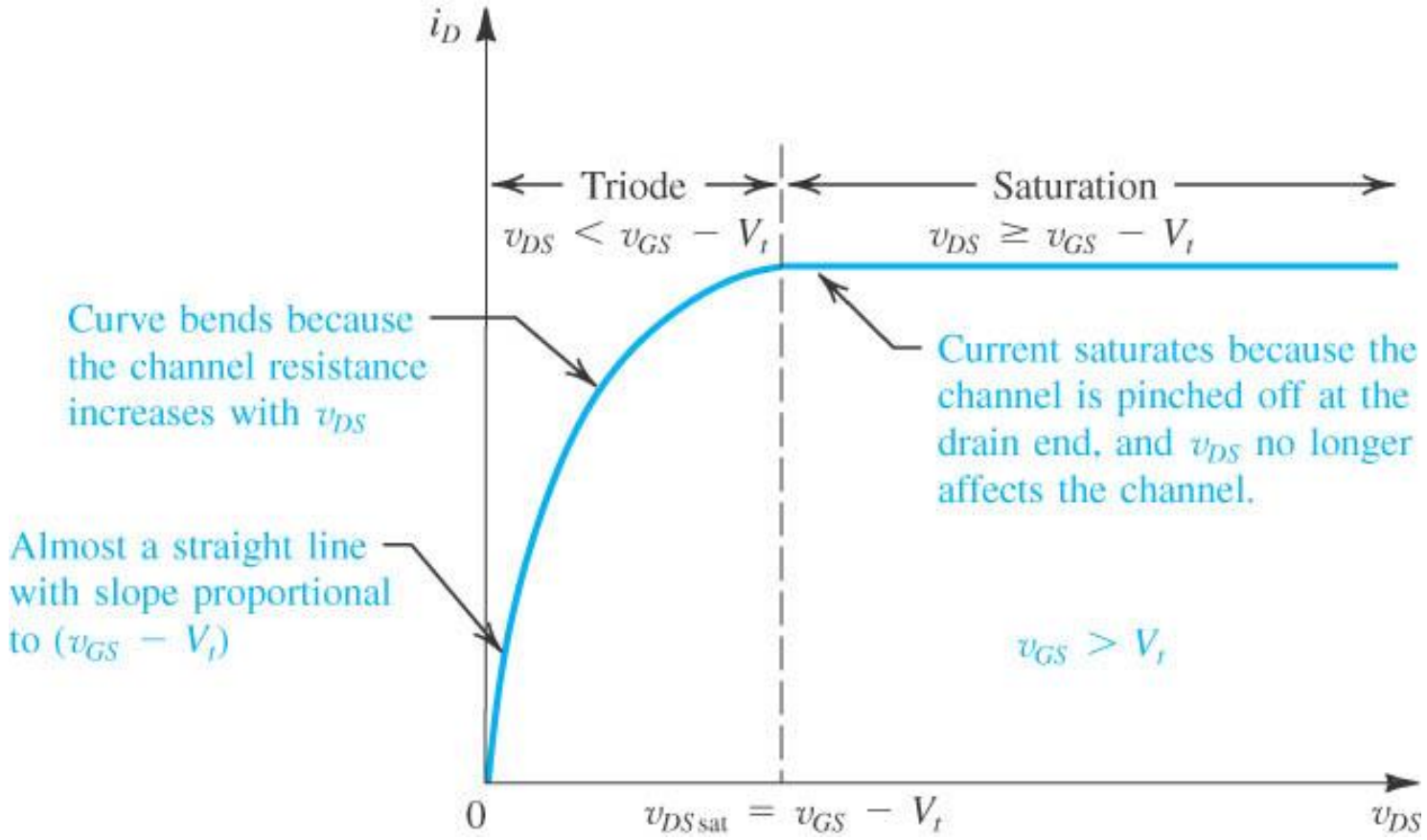


Figure 7. The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$.

How MOSFET Works

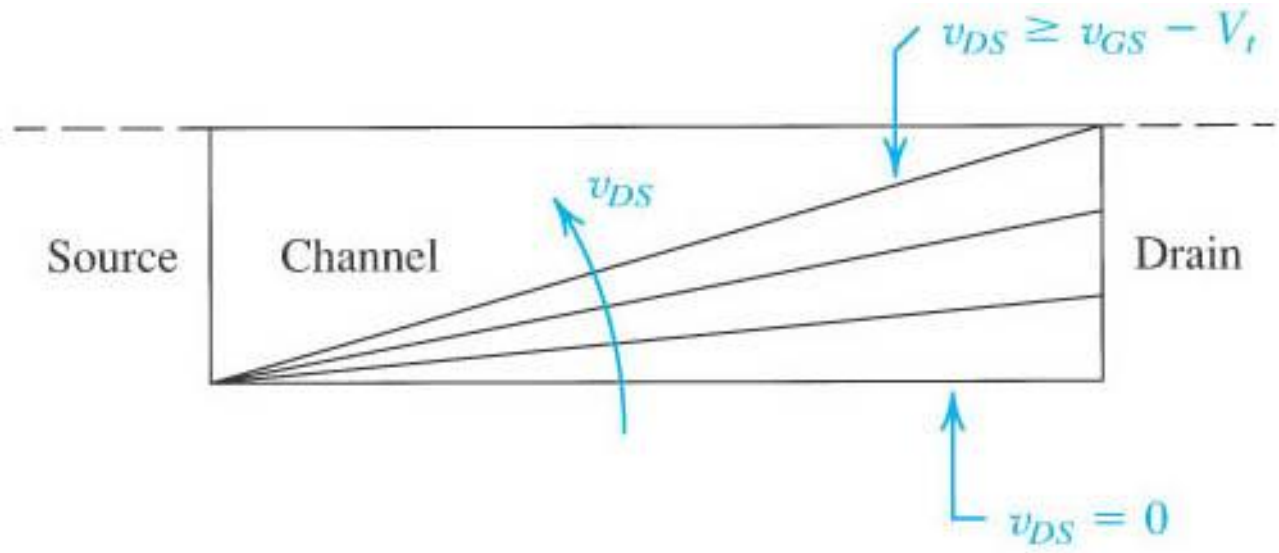


Figure 8. Increasing v_{DS} causes the channel to acquire a tapered shape. Eventually, as v_{DS} reaches $v_{GS} - V_t$, the channel is pinched off at the drain end. Increasing v_{DS} above $v_{GS} - V_t$ has little effect (theoretically, no effect) on the channel's shape.

How MOSFET Works

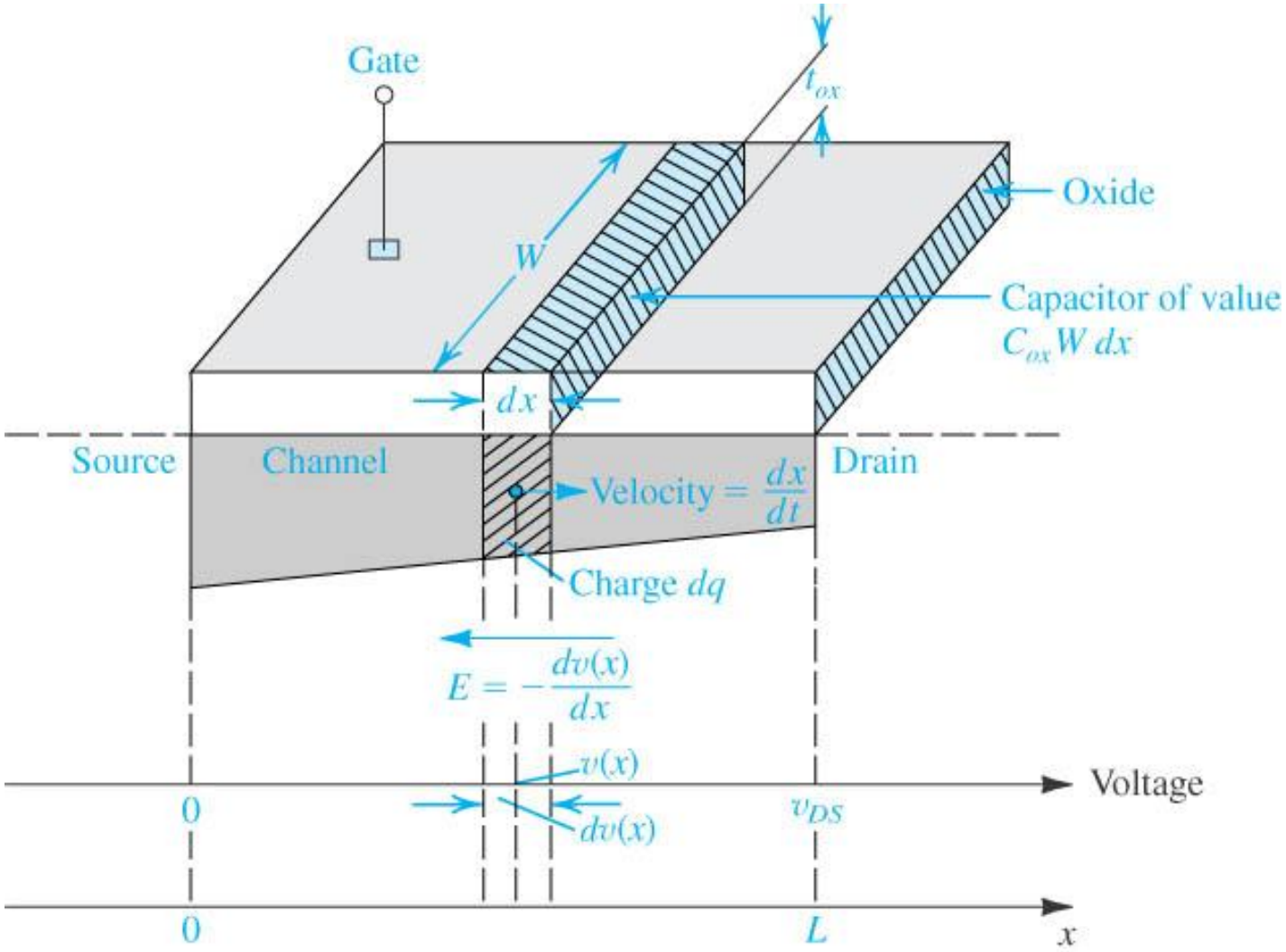
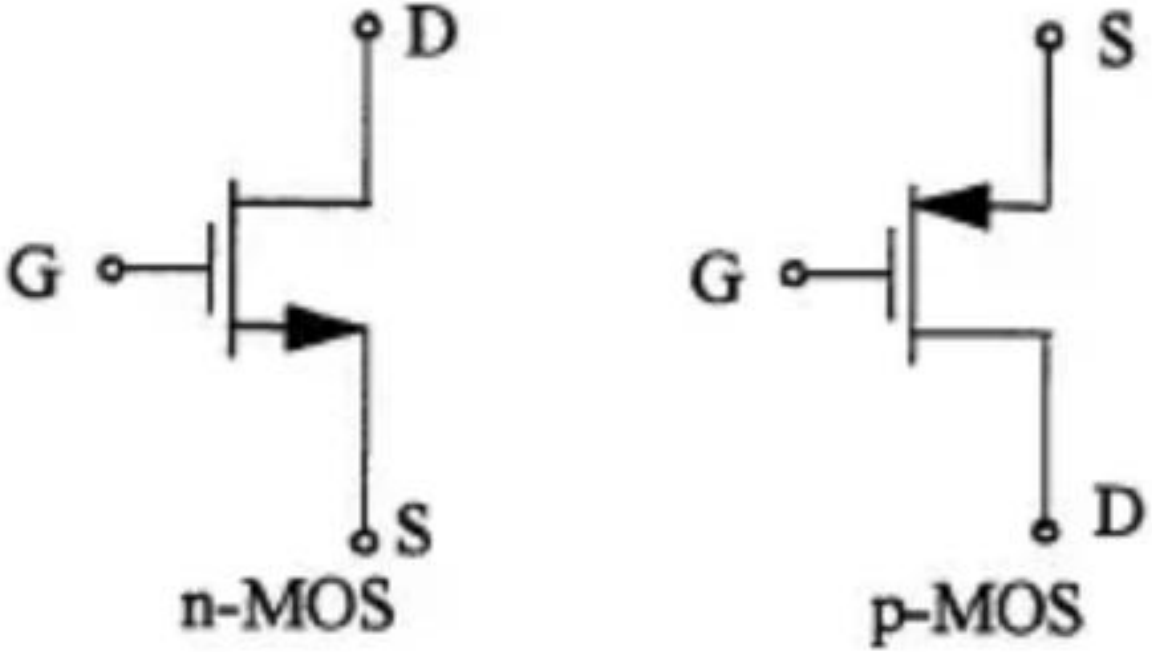


Figure 9. Derivation of the i_D–v_{DS} characteristic of the NMOS transistor.

NMOS vs PMOS



NMOS vs PMOS

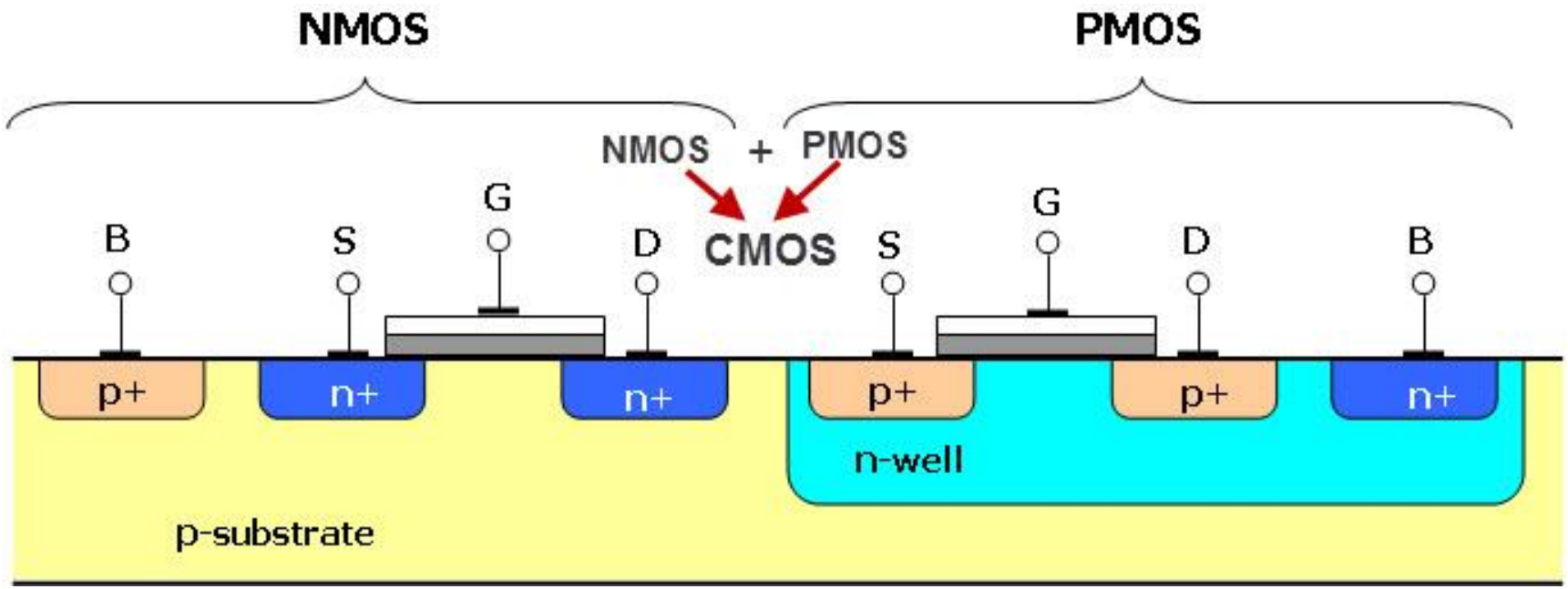


Figure 10. Cross-section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate *n*-type region, known as an *n* well. Another arrangement is also possible in which an *n*-type body is used and the *n* device is formed in a *p* well. Not shown are the connections made to the *p*-type body and to the *n* well; the latter functions as the body terminal for the *p*-channel device.

NMOS vs PMOS

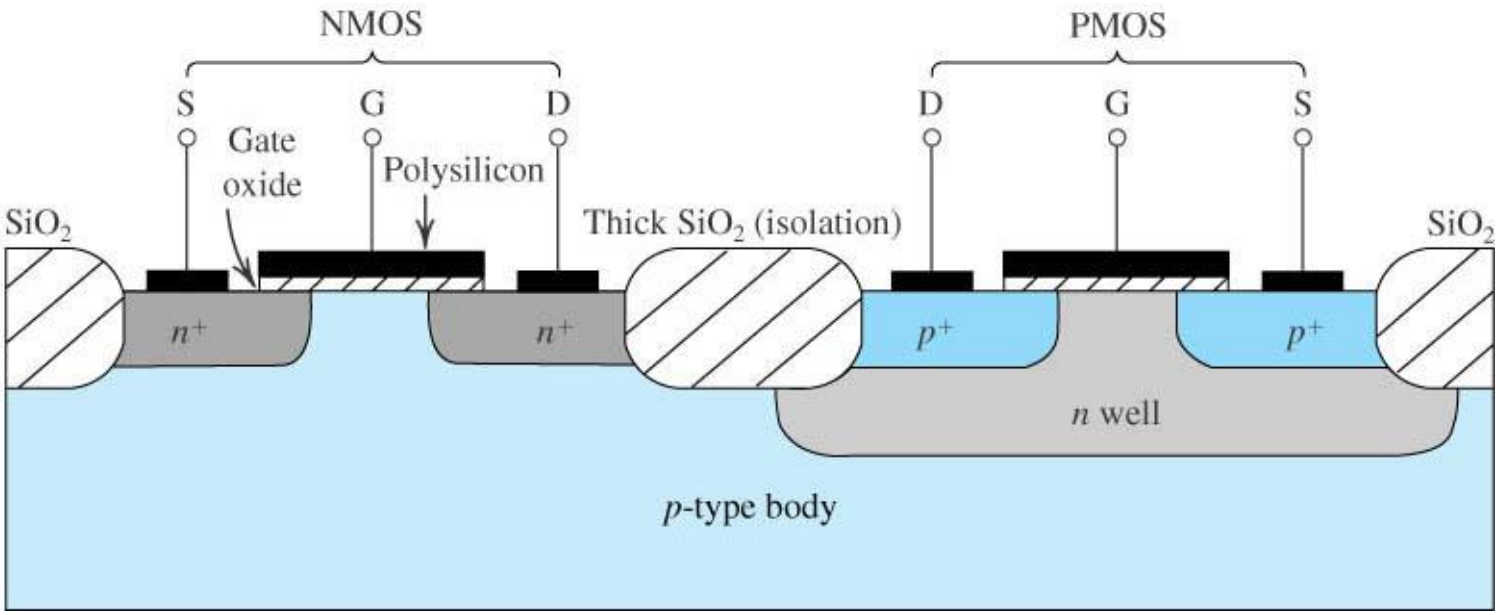
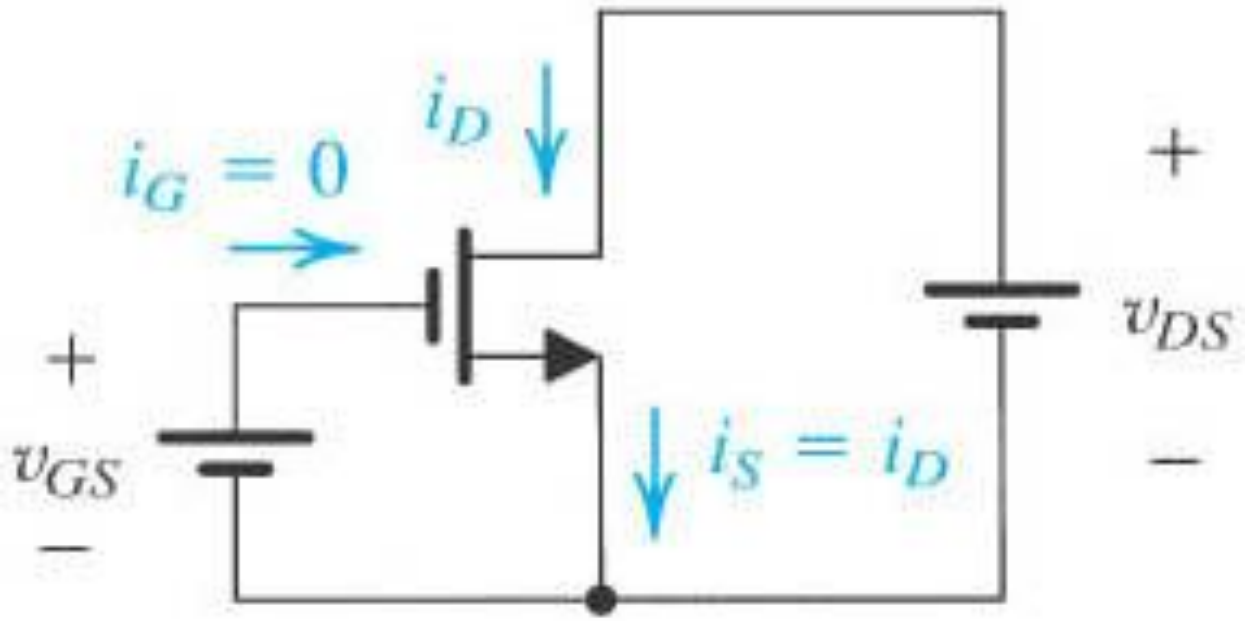


Figure 11. Cross-section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate *n*-type region, known as an *n* well. Another arrangement is also possible in which an *n*-type body is used and the *n* device is formed in a *p* well. Not shown are the connections made to the *p*-type body and to the *n* well; the latter functions as the body terminal for the *p*-channel device.

Biasing MOSFET



Biasing MOSFET

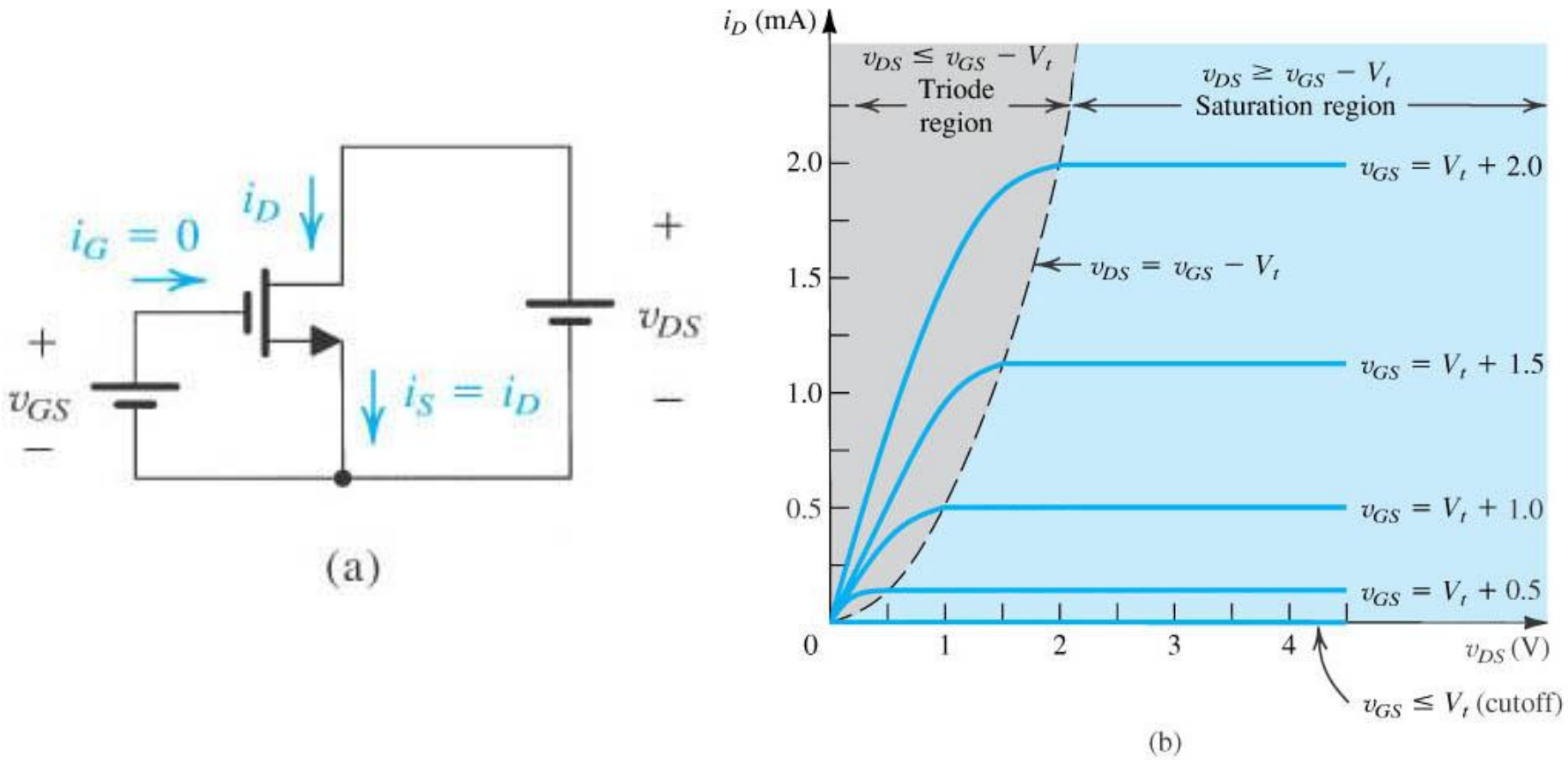


Figure 12. **(a)** An *n*-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. **(b)** The i_D–v_{DS} characteristics for a device with $k'_n(W/L) = 1.0$ mA/V^2.

Biasing MOSFET

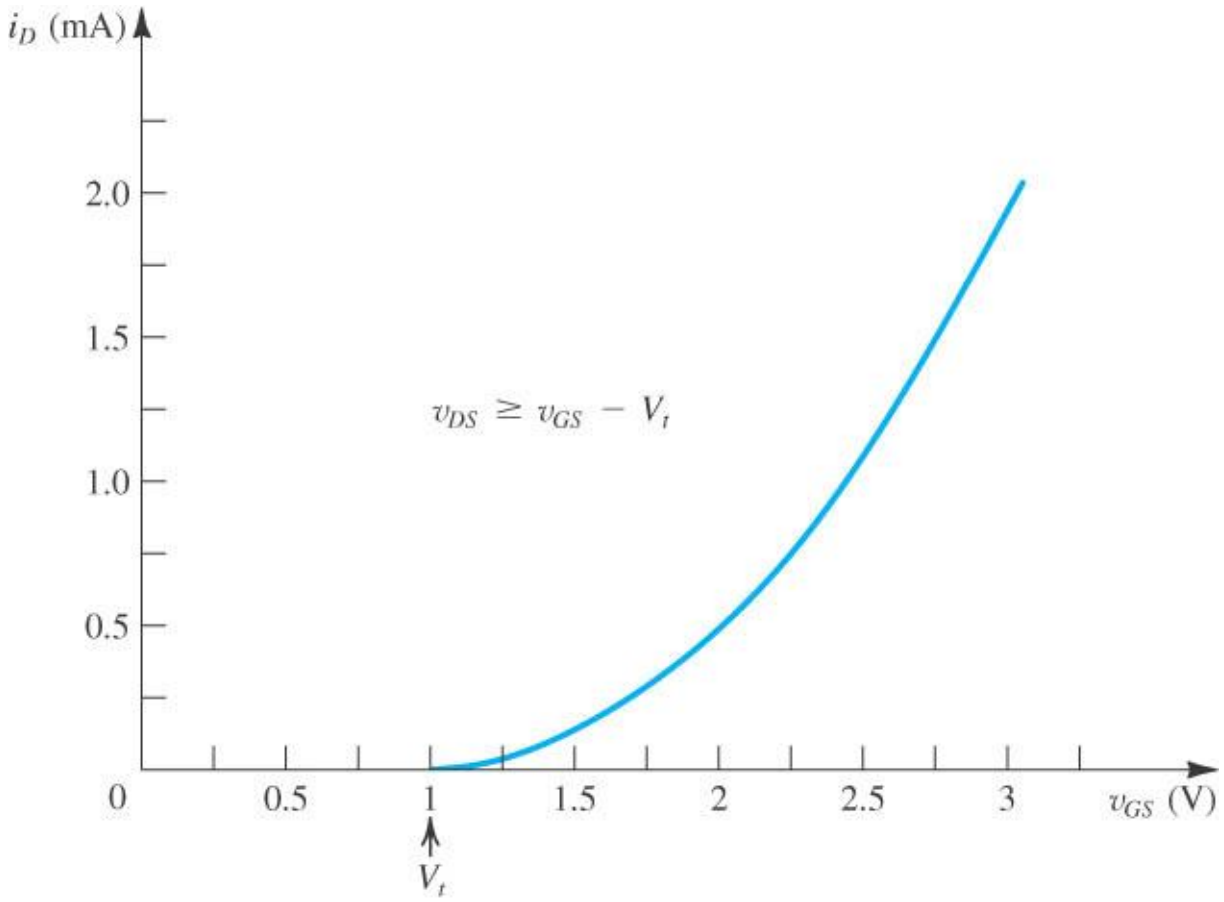


Figure 13. The i_D–v_{GS} characteristic for an enhancement-type NMOS transistor in saturation (V_t = 1 V, k'_n W/L = 1.0 mA/V^2).

Biasing MOSFET

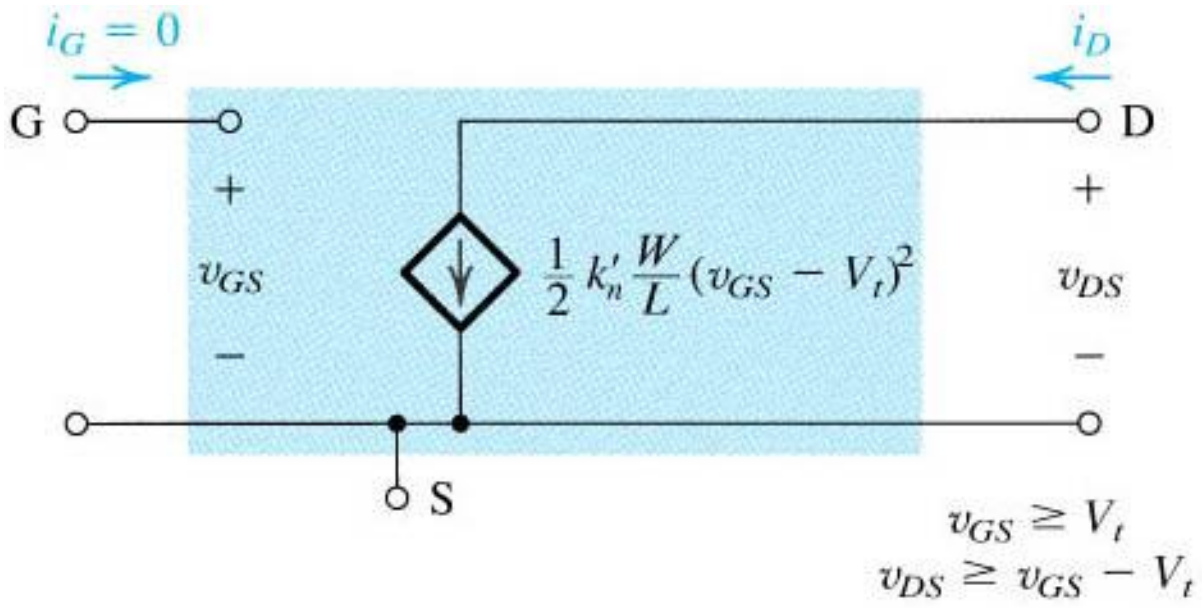


Figure 14. Large-signal equivalent-circuit model of an *n*-channel MOSFET operating in the saturation region.

Biasing MOSFET

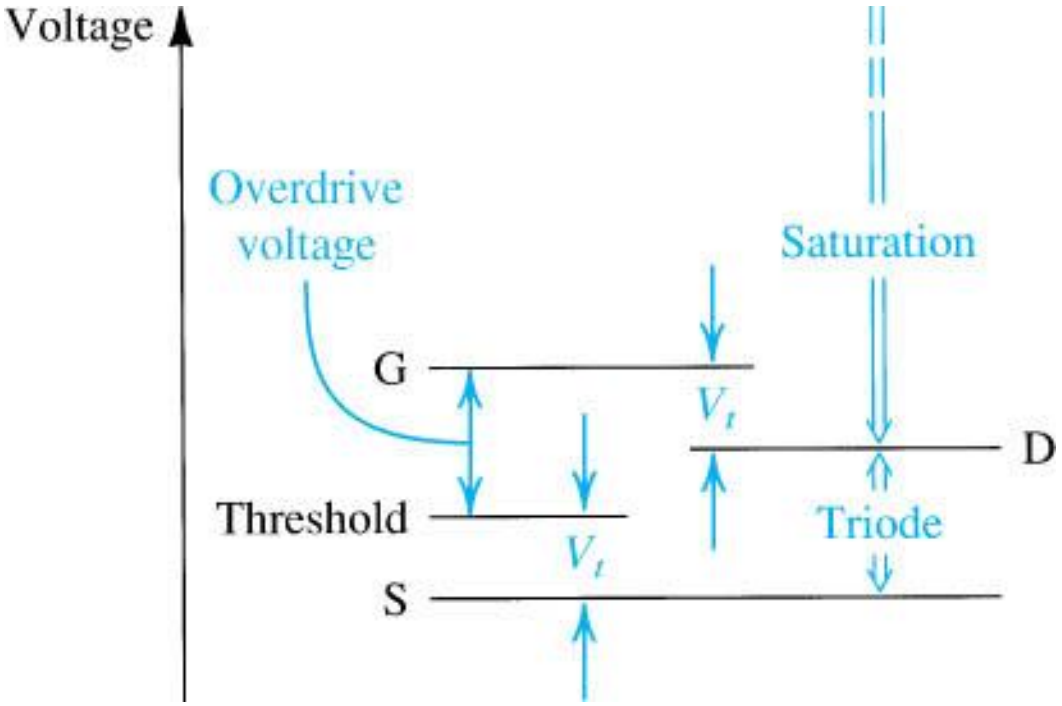
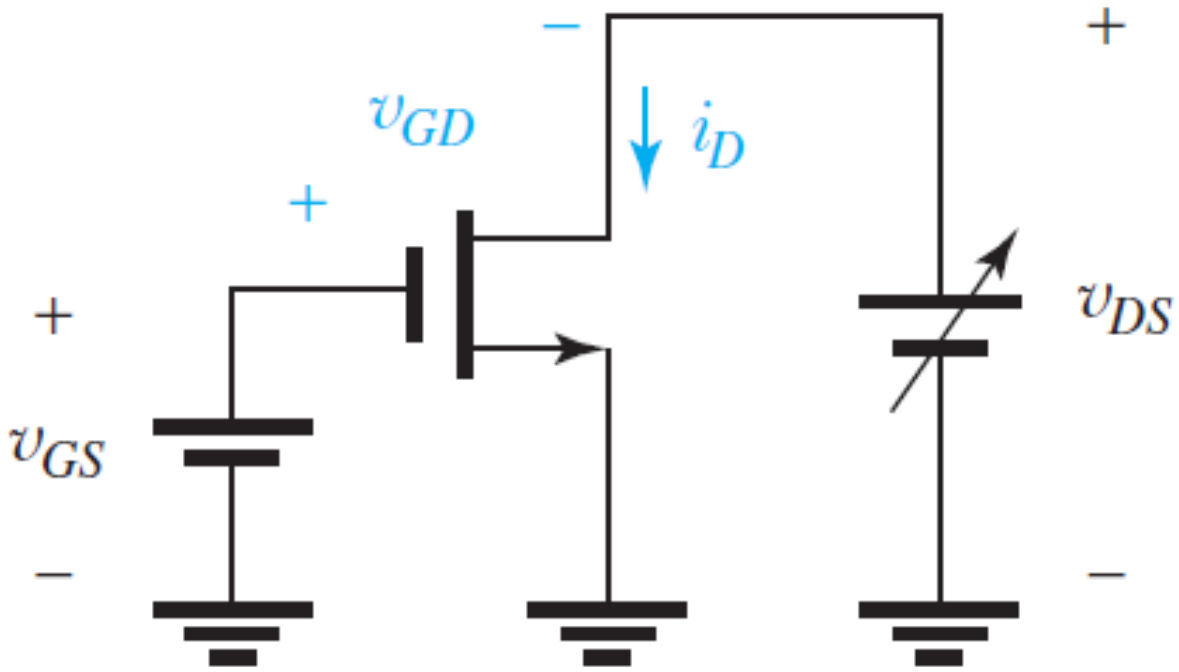


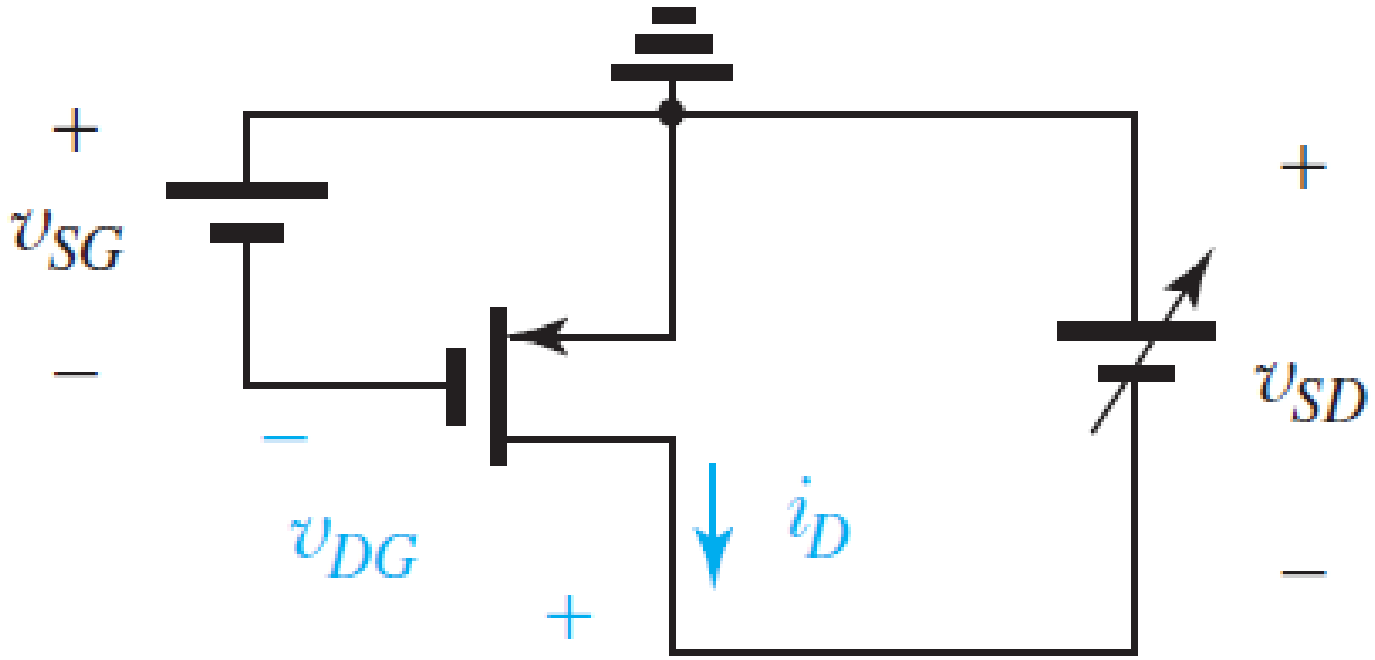
Figure 15. The relative levels of the terminal voltages of the enhancement NMOS transistor for operation in the triode region and in the saturation region.

NMOS Transistor



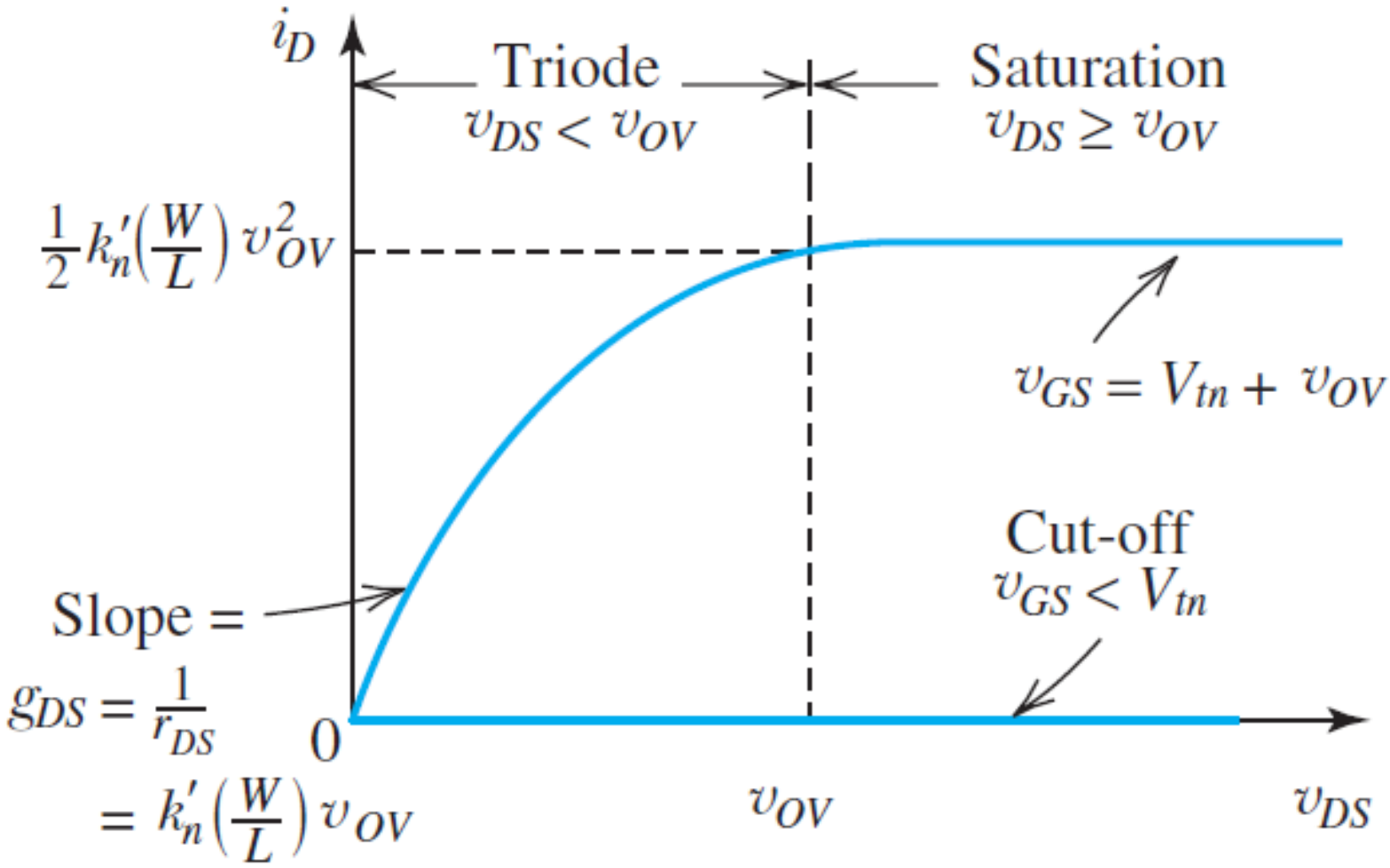
Biasing MOSFET

PMOS Transistor



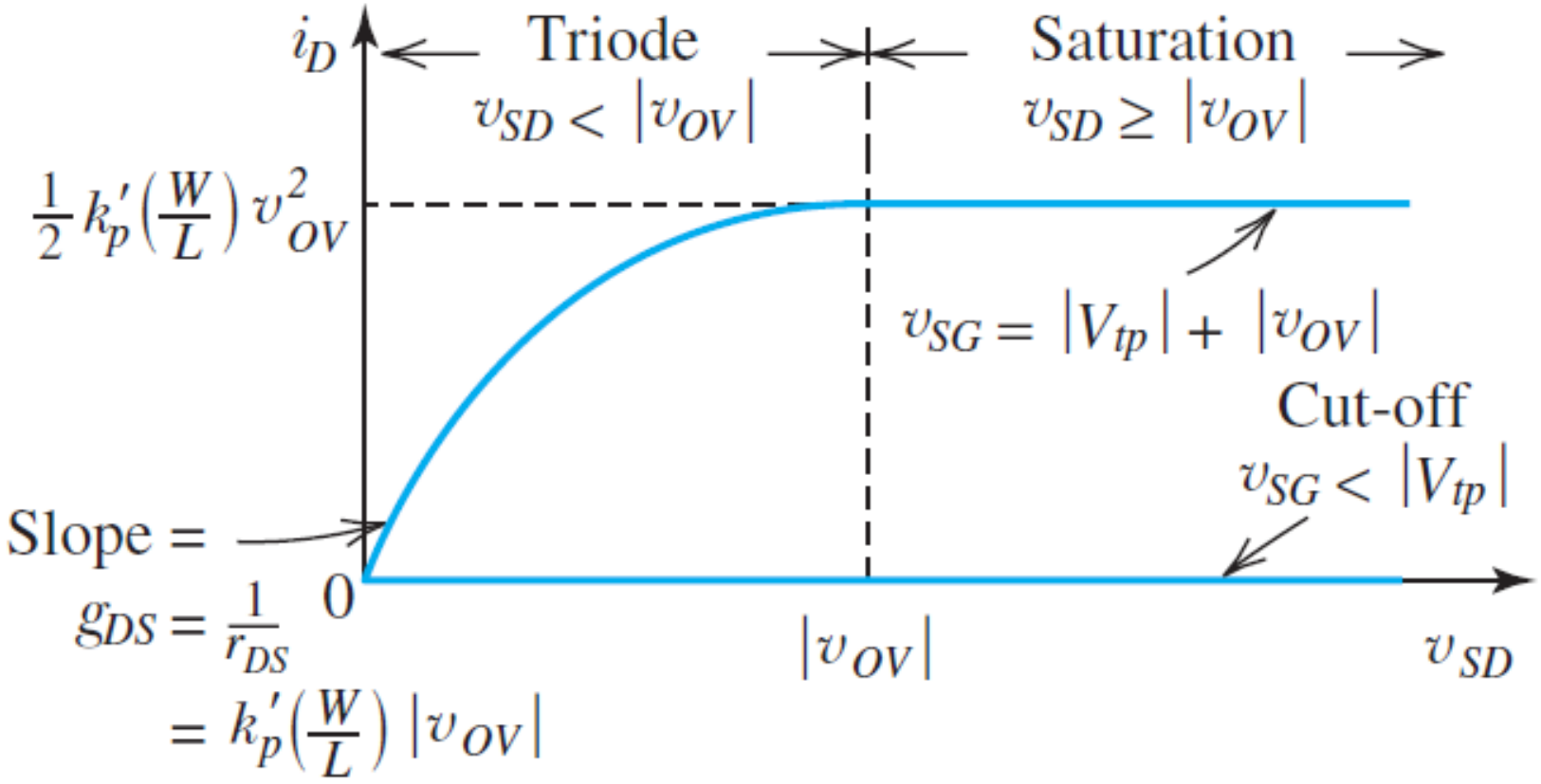
Mode of Operation

NMOS Transistor



Mode of Operation

PMOS Transistor



Mode of Operation

For NMOS transistor :

$V_{OV} = V_{GS} - V_{tn}$

For PMOS transistor :

$|V_{OV}| = V_{SG} - V_{tp}$

MOSFET Equation

Cut-off: $V_{GS} < V_T$

$$I_D = I_S = 0$$

Triode: $V_{GS} > V_T$ and $V_{DS} < V_{GS} - V_T$

$$I_D = k_n'(W/L)[(V_{GS}-V_T)V_{DS} - {}^1/_2 V_{DS}^2]$$

Saturation: $V_{GS} > V_T$ and $V_{DS} > V_{GS} - V_T$

$$I_D = {}^1/_2 k_n'(W/L)(V_{GS}-V_T)^2$$

where k_n' = (electron mobility)x(gate capacitance)

$$= \mu_n C_{ox} \quad \text{...electron velocity} = \mu_n \boldsymbol{E}$$

and V_T depends on the doping concentration and gate material used

MOSFET Equation

NMOS Transistor

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leqslant V_{tn}$$

or equivalently:

$$v_{DS} \geqslant v_{OV}$$

Then

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently,

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

MOSFET Equation

PMOS Transistor

Triode Region

Continuous channel, obtained by:

$$v_{DG} > |V_{tp}|$$

or equivalently:

$$v_{SD} < |v_{OV}|$$

Then,

$$i_D = k_p'\left(\frac{W}{L}\right)\left[(v_{SG} - |V_{tp}|)v_{SD} - \frac{1}{2}v_{SD}^2\right]$$

or equivalently

$$i_D = k_p'\left(\frac{W}{L}\right)\left(|v_{OV}| - \frac{1}{2}v_{SD}\right)v_{SD}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{DG} \leqslant |V_{tp}|$$

or equivalently

$$v_{SD} \geqslant |v_{OV}|$$

Then

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(v_{SG} - |V_{tp}|)^2$$

or equivalently

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)v_{OV}^2$$

Example

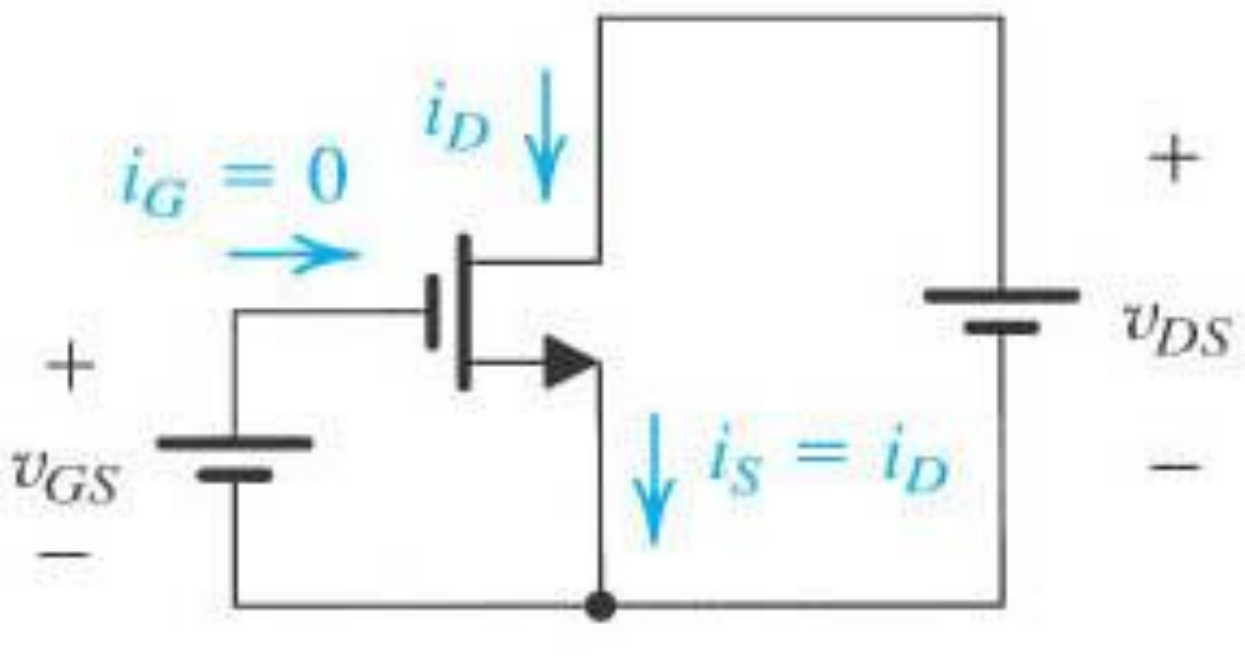
Consider an NMOS transistor with V_t = 0.7 V, k_n' = 194 µA/V^2, W = 8 µm, and L = 0.8 µm.

a. Calculate the values of V_{OV}, V_{GS}, and V_{DSmin} needed to operate the transistor in the saturation region with a DC current I_D = 100 µA.

b. Calculate the values of V_{DS} when V_{GS} remain constant that results in I_D = 60 µA.

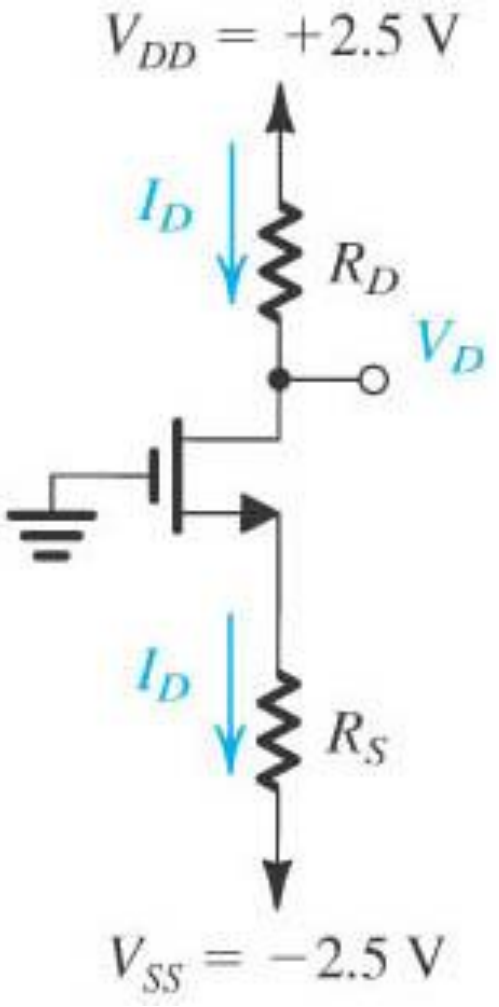
Biasing MOSFET

There are some ways to bias the MOSFET. The most common ways :



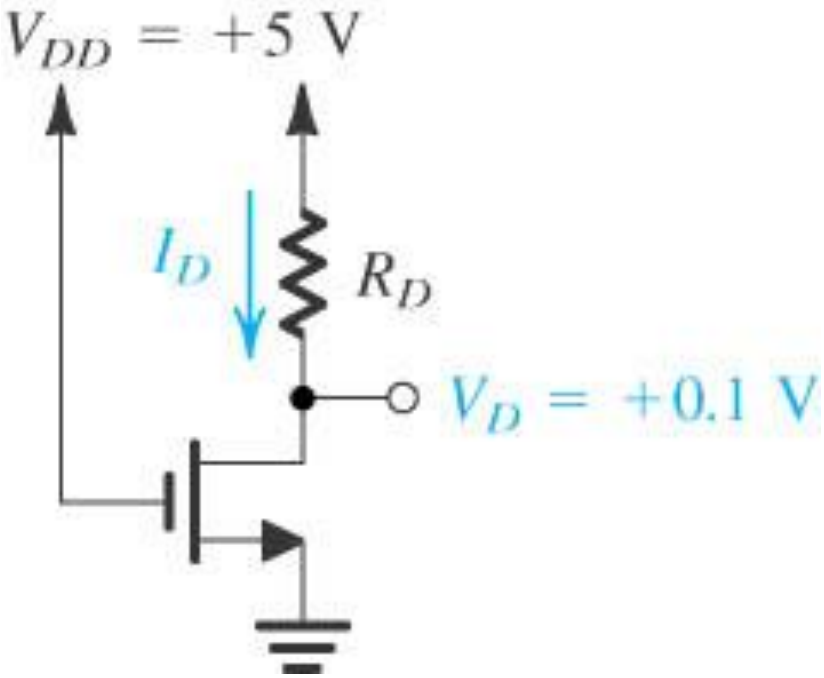
Example

Determine the values of R_D and R_S so that the transistor operates at I_D = 0.4 mA and V_D = +0.5 V. The NMOS transistor has V_t = 0.7 V, $\mu_n C_{ox}$ = 100 μA/V^2, L = 1 μm, and W = 32 μm.



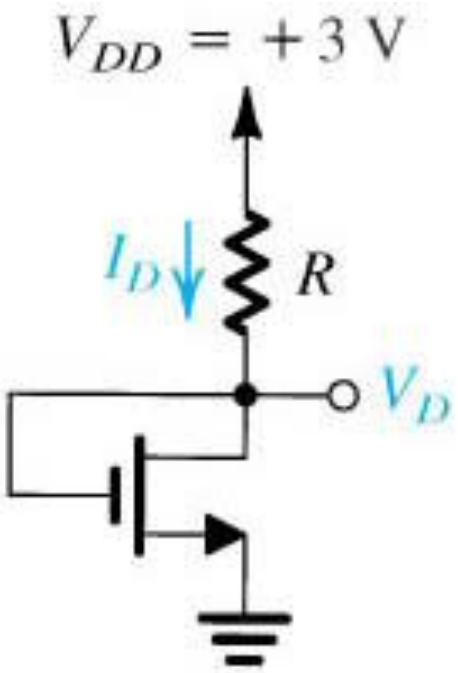
Example

Determine the values of I_D and R_D to establish a drain voltage of 0.1 V. Knowing the NMOS transistor has V_t = 1 V and k_n = 1 mA/V^2.



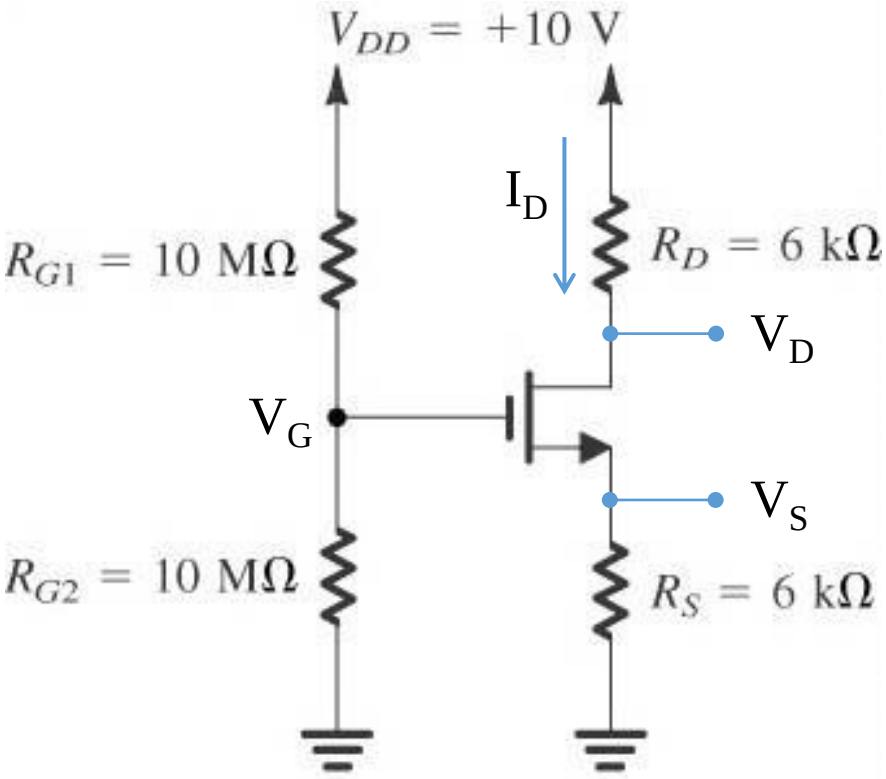
Example

Determine the values of R so that the transistor operates at $V_D = 0.8$ V. Knowing the NMOS transistor has $V_t = 0.5$ V and $k_n = 1.6$ mA/V^2.

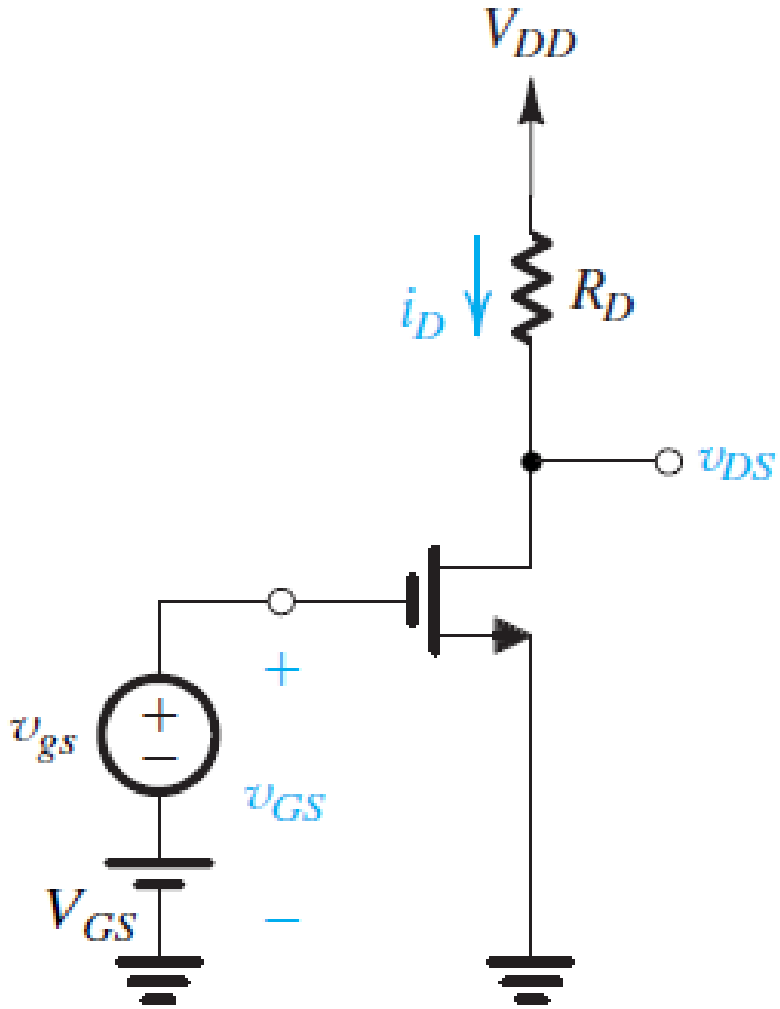


Example

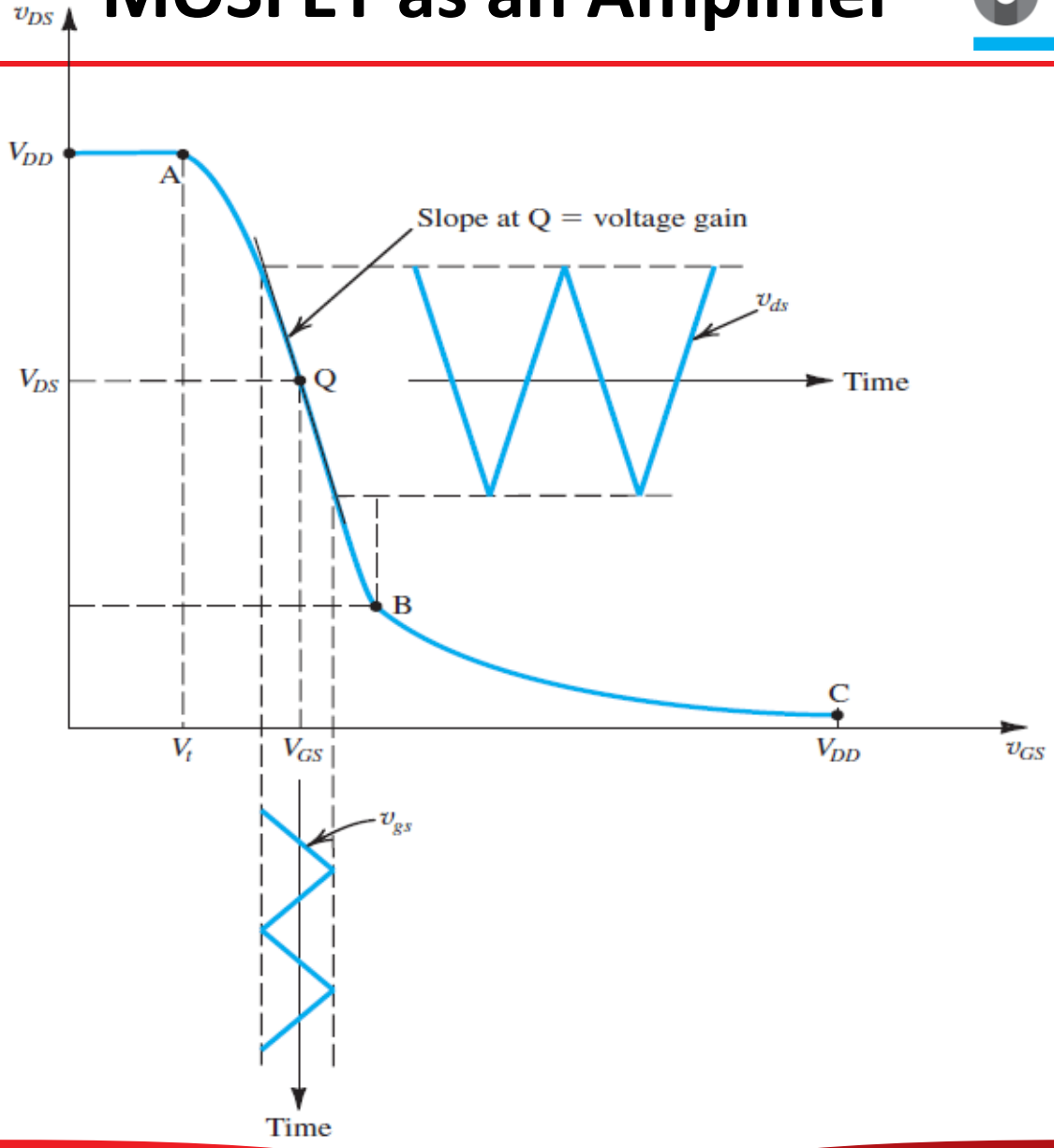
Determine the values of I_D, V_D, V_G, and V_S. The NMOS transistor has V_t = 1 V, k_n = 1 mA/V^2.



MOSFET as an Amplifier



MOSFET as an Amplifier

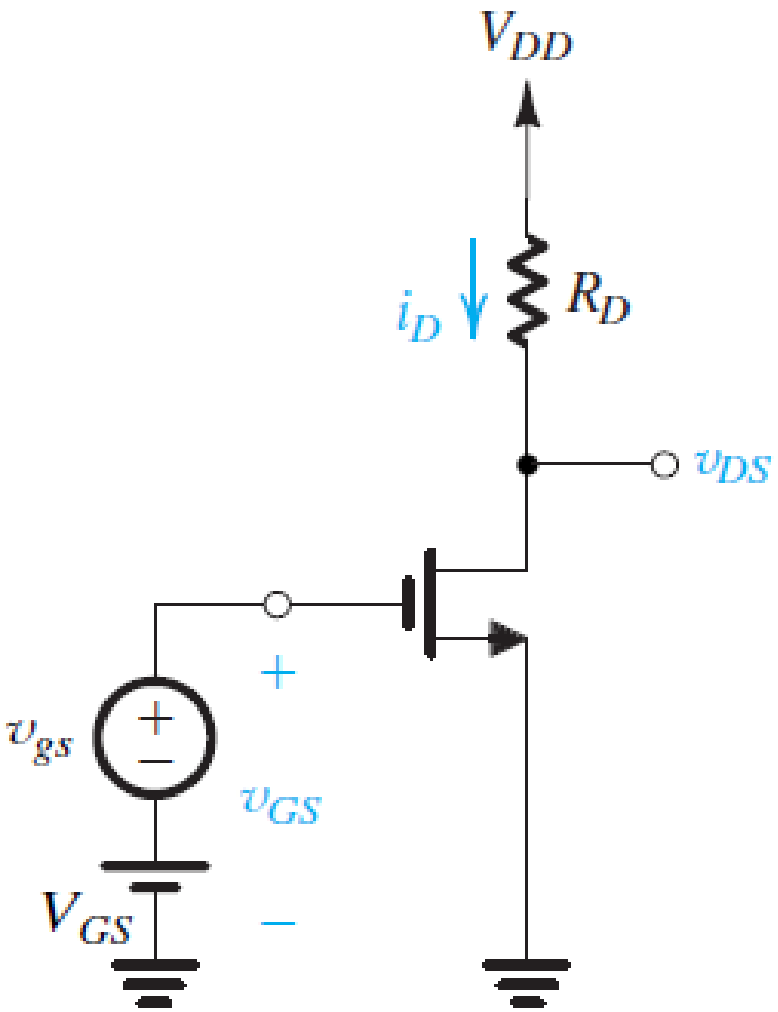


MOSFET as an Amplifier

Jika diketahui:

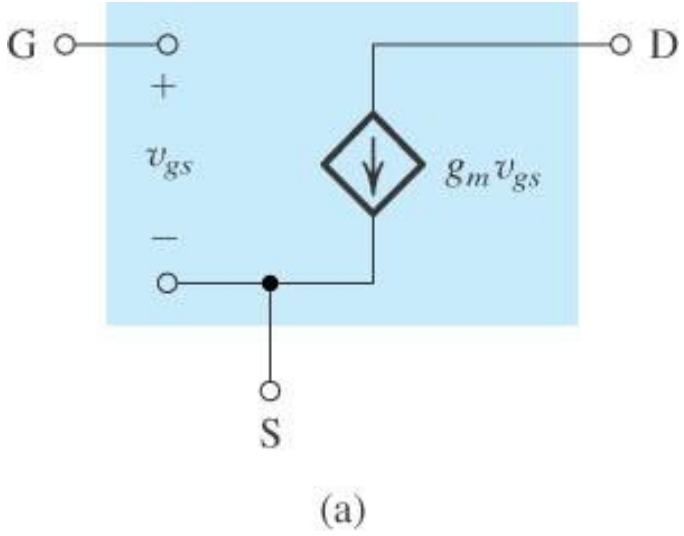
$V_t = 0.4$ V,
$k_n = 4$ mA/V^2,
$V_{DD} = 1.8$ V,
$R_D = 17.5$ kΩ,
$V_{GS} = 0.6$ V,

a. Tentukan V_{OV}, I_D, dan V_{DS} , jika $v_{gs} = 0$ V
b. Hitung kembali V_{DS} jika v_{gs} berubah sebesar $\pm$5 mV
c. Tentukan besar penguatan A_v



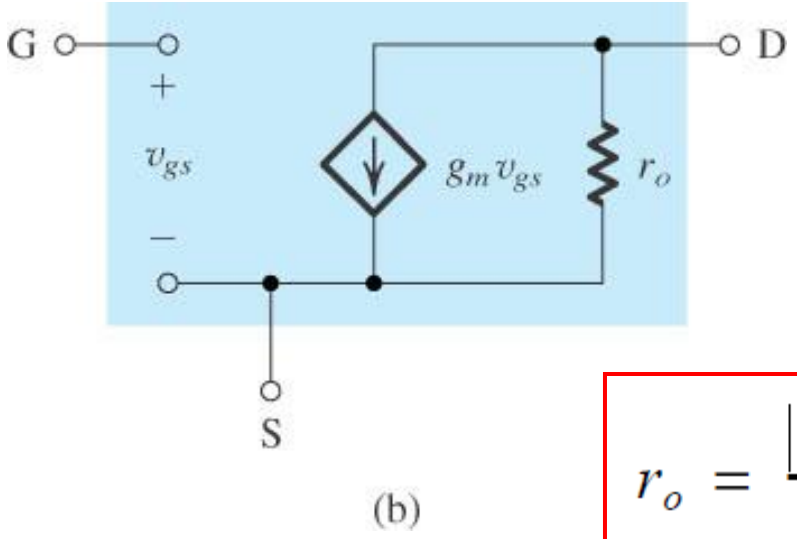
Small-signal Model

Jika *tidak* memiliki nilai V_A :



(a)

Jika memiliki nilai V_A :



(b)

$$r_o = \frac{|V_A|}{I_D}$$

$$g_m = k_n'(W/L)\,(V_{GS} - V_t) = k_n\,V_{OV}$$
$$= k_n\,V_{OV}$$

Small-signal Analysis

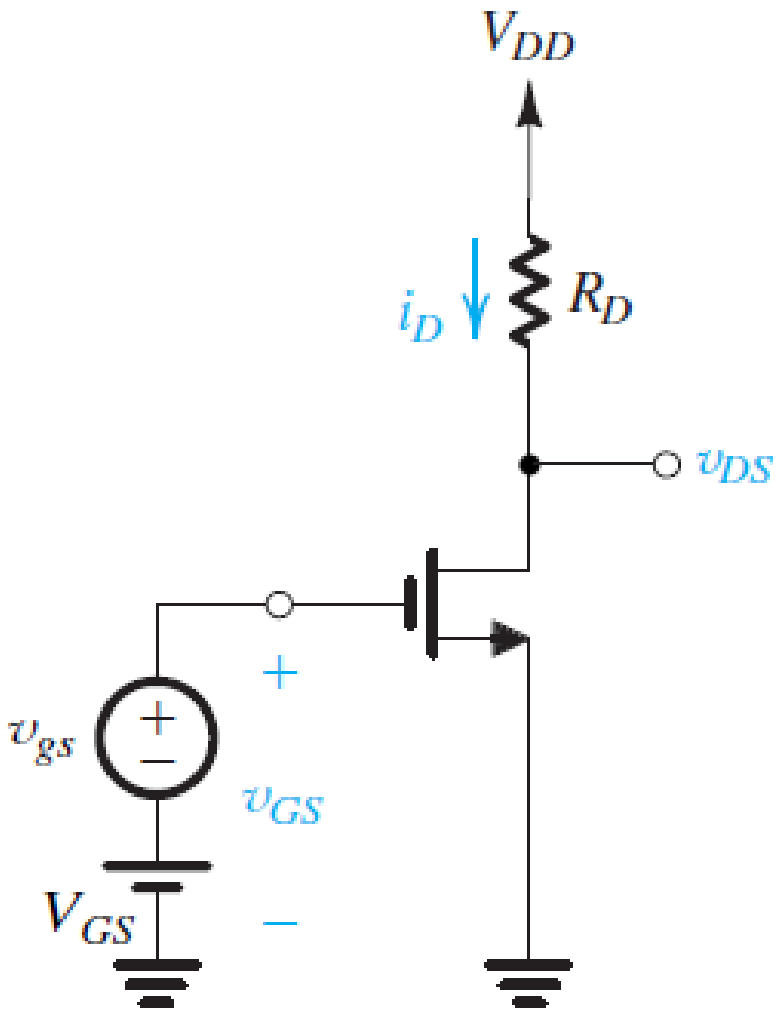
1. Analisis rangkaian secara DC, (bila ada) kapasitor menjadi open-circuit.
2. Tentukan nilai V_G, V_S, V_D, dan I_D.
3. Tentukan nilai g_m dan r_o (bila ada).
4. Analisis rangkaian secara AC, sumber tegangan DC dan (bila ada) kapasitor menjadi short-circuit.
5. Ganti MOSFET dengan model pengganti sinyal kecil.
6. Tentukan nilai A_V (v_o / v_{gs}).

Small-signal Analysis

Jika diketahui:

$V_t = 0.4$ V
$k_n = 4$ mA/V^2
$V_{DD} = 1.8$ V
$R_D = 17.5$ kΩ
$V_{GS} = 0.6$ V

a. Tentukan V_{OV}, I_D, dan V_{DS} , jika $v_{gs} = 0$ V
b. Tentukan besar penguatan A_v dengan analisis sinyal kecil



Small-signal Analysis

Step 1

Hitung nilai V_{OV}, I_D, V_{DS}, g_m dan r_o

$$V_{OV} = 0.6 - 0.4$$

$$V_{OV} = 0.2 \text{ volt}$$

$$I_D = \frac{1}{2} k_n V_{OV}^{\ 2}$$

$$I_D = \frac{1}{2} \times 4 \times (0.2)^2$$

$$I_D = 0.08 \text{ mA}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{DS} = 1.8 - (0.08 \times 17.5)$$

$$V_{DS} = 0.4 \text{ volt}$$

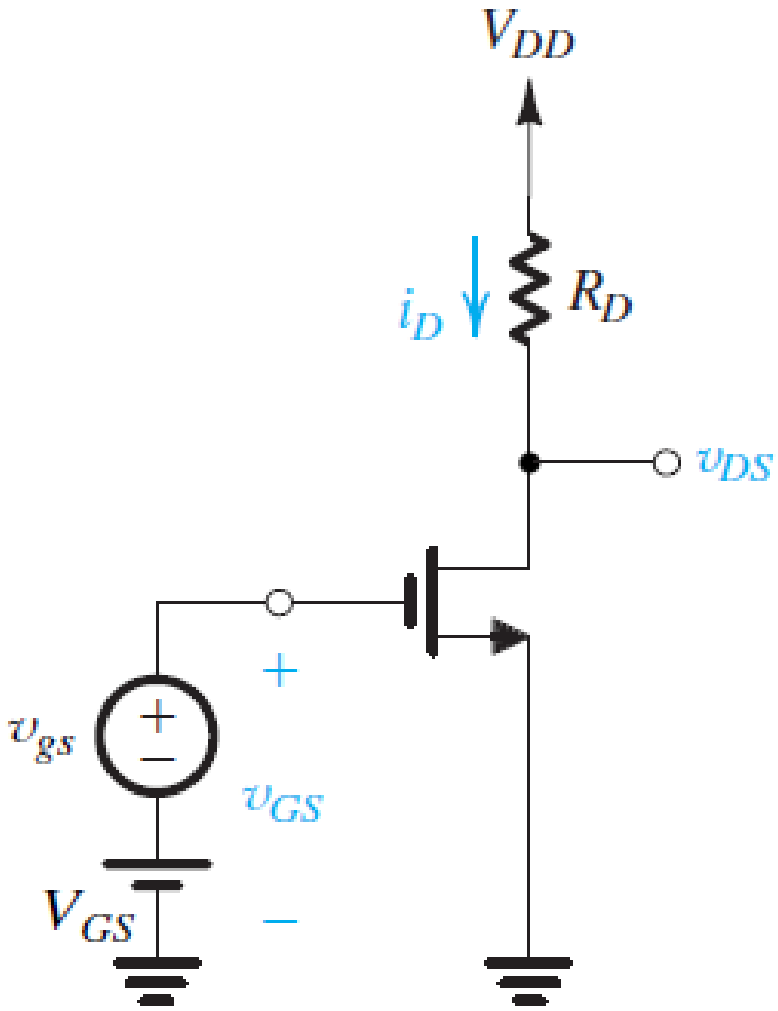
$$g_m = k_n V_{OV}$$

$$g_m = 4 \times 0.2 = 0.8 \text{ mA/V}$$

Small-signal Analysis

Step 2

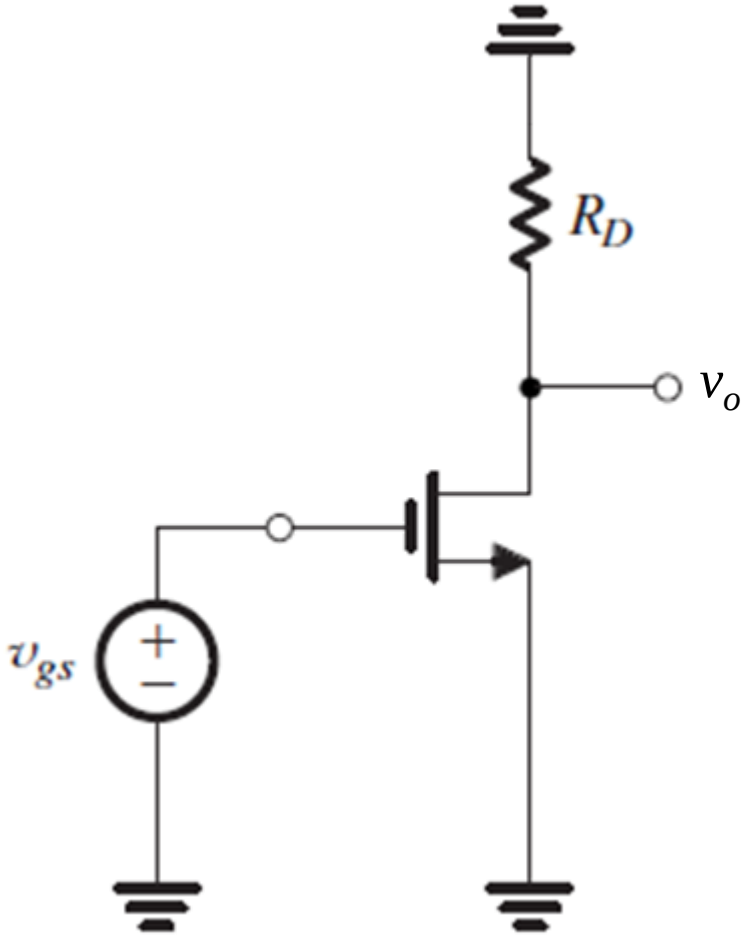
Hilangkan sumber DC
(jadikan short circuit)



Small-signal Analysis

Step 2

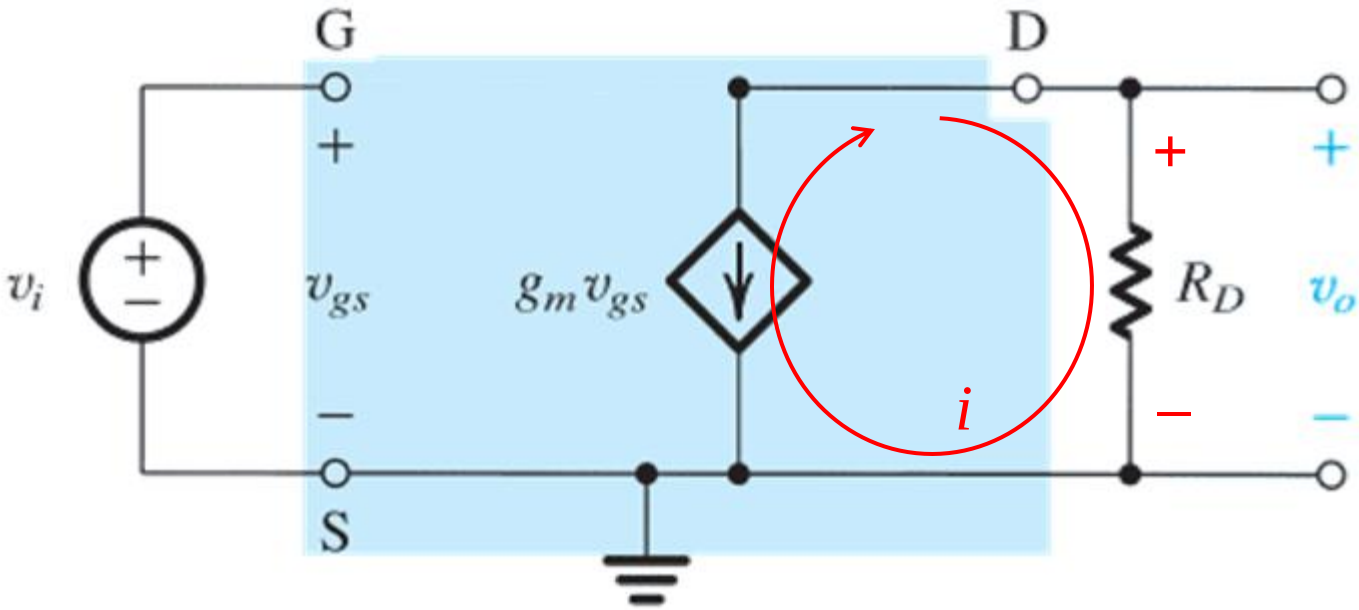
Hilangkan sumber DC
(jadikan short circuit)



Small-signal Analysis

Step 3

Ubah menjadi model sinyal kecil



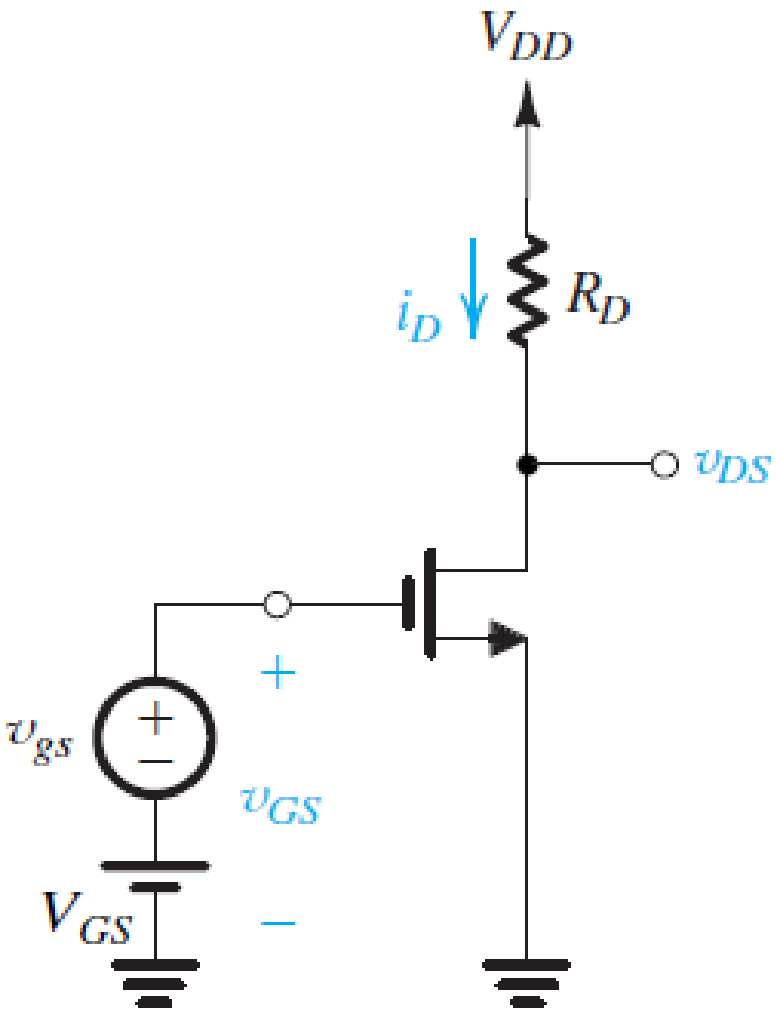
Homework

Jika diketahui:

$V_t = 0.4$ V
$k_n = 4$ mA/V^2
$V_{DD} = 1.8$ V
$R_D = 17.5$ kΩ
$V_{GS} = 0.6$ V

$V_A = 50$ V

Tentukan besar penguatan A_v dengan analisis sinyal kecil



Solution

Step 1

Hitung nilai V_{OV}, I_D, V_{DS}, g_m dan r_o

$$V_{OV} = 0.6 - 0.4$$

$$V_{OV} = 0.2 \text{ volt}$$

$$I_D = \frac{1}{2} k_n V_{OV}^{\ 2}$$

$$I_D = \frac{1}{2} \times 4 \times (0.2)^2$$

$$I_D = 0.08 \text{ mA}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{DS} = 1.8 - (0.08 \times 17.5)$$

$$V_{DS} = 0.4 \text{ volt}$$

$$g_m = k_n V_{OV}$$

$$g_m = 4 \times 0.2 = 0.8 \text{ mA/V}$$

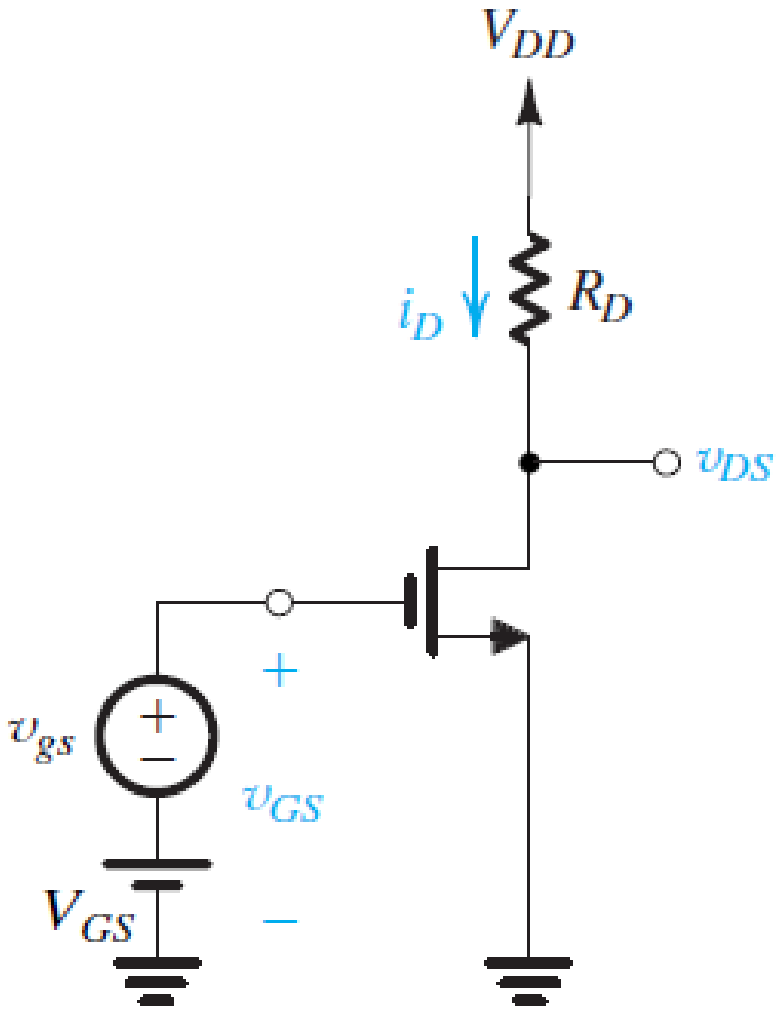
$$r_o = \frac{V_A}{I_D}$$

$$r_o = \frac{50}{0.08} = 625\,\Omega$$

Solution

Step 2

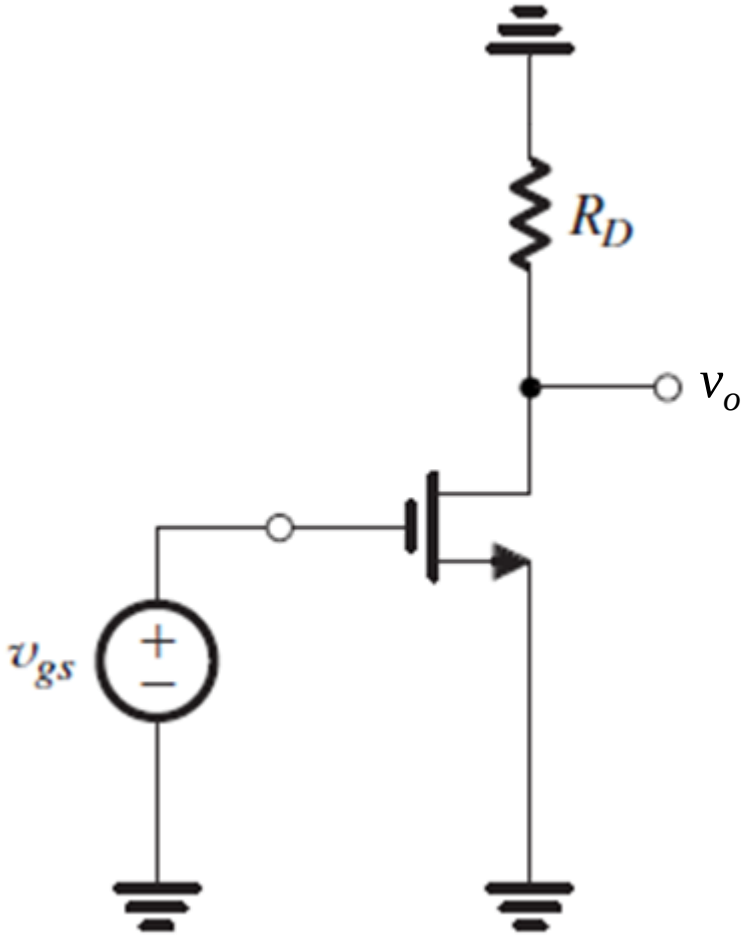
Hilangkan sumber DC
(jadikan short circuit)



Solution

Step 2

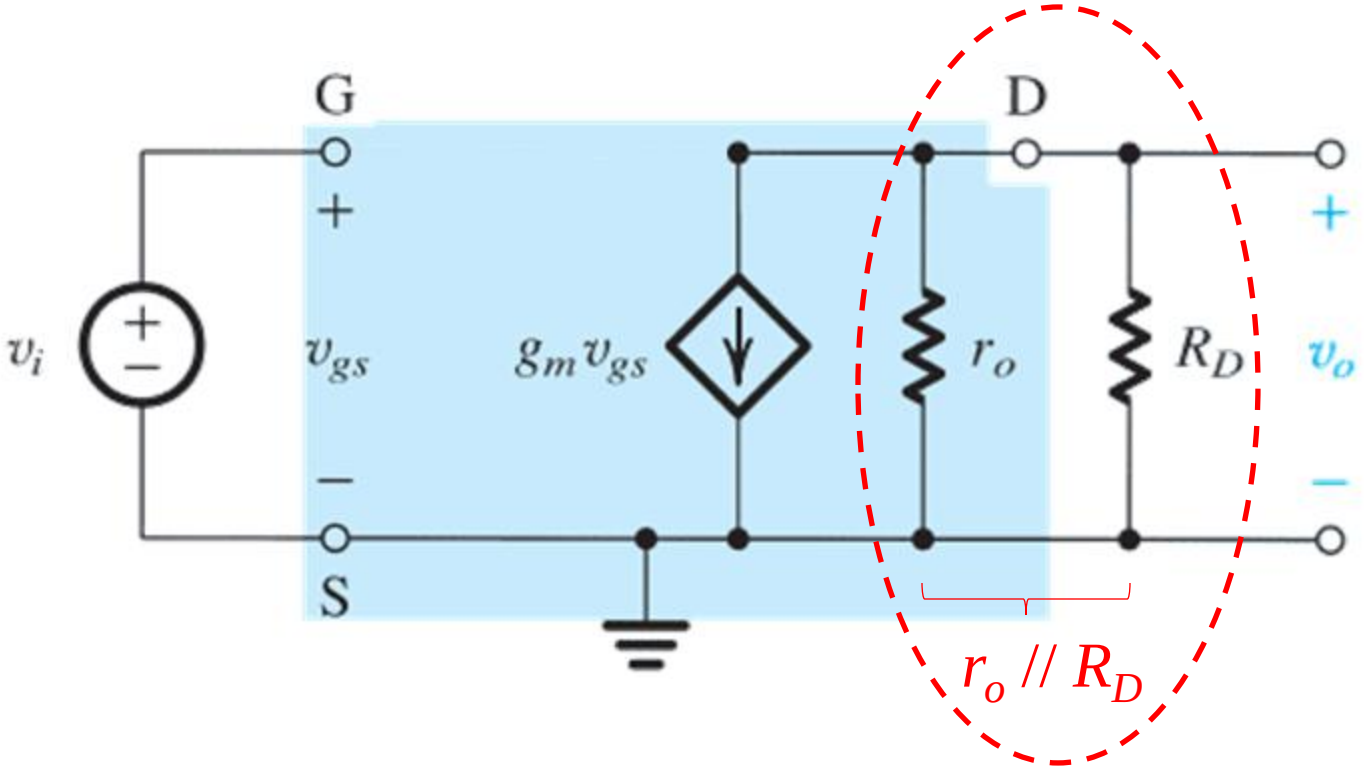
Hilangkan sumber DC
(jadikan short circuit)



Solution

Step 3

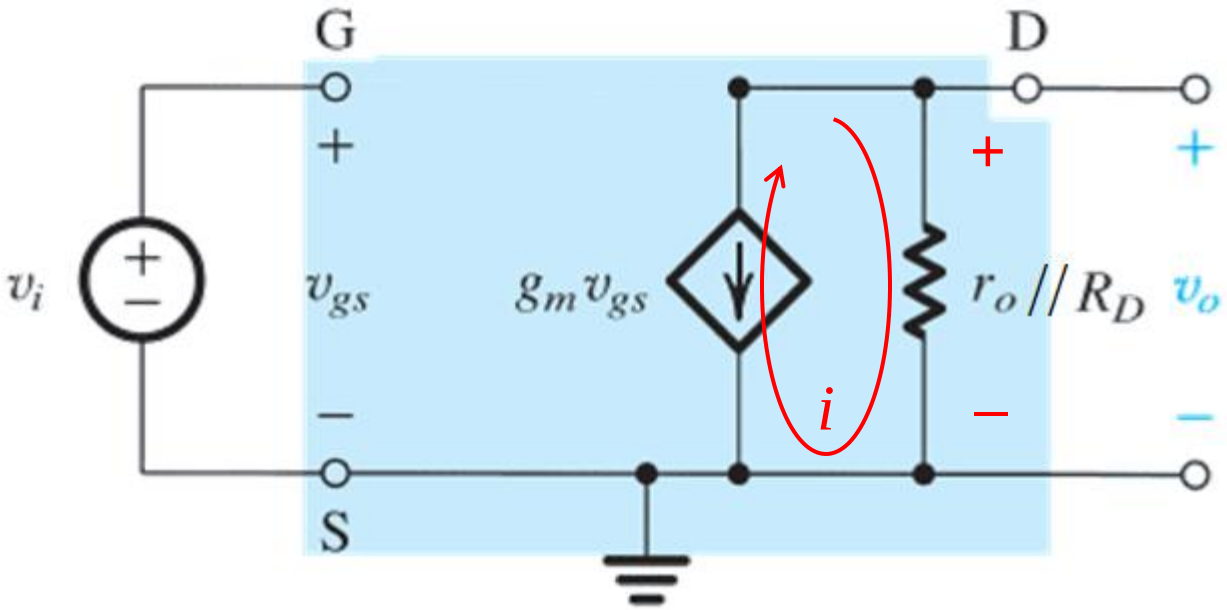
Ubah menjadi model sinyal kecil



Solution

Step 3

Ubah menjadi model sinyal kecil



$$v_o = i \times R$$
$$= -g_m v_{gs} \times (r_o // R_D)$$


рахмат
danke
謝謝
ngiyabonga
Баярлалаа
spas
teşekkür ederim
mersi
kia ora
barka
welalin
tack
спасибо
faafetai lava
vinaka
спасибі
blagodaram
dank je
misaotra
matondo
paldies
grazzi
mahalo
tapadh leat
kiitos
dankie
nanni
nandri
dhanyavad
thank you
gracias
хвала
asante
manana
obrigada
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bedankt
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rahmat
ευχαριστώ
তোমাকে ধন্যবাদ
감사합니다
xiexie
merci