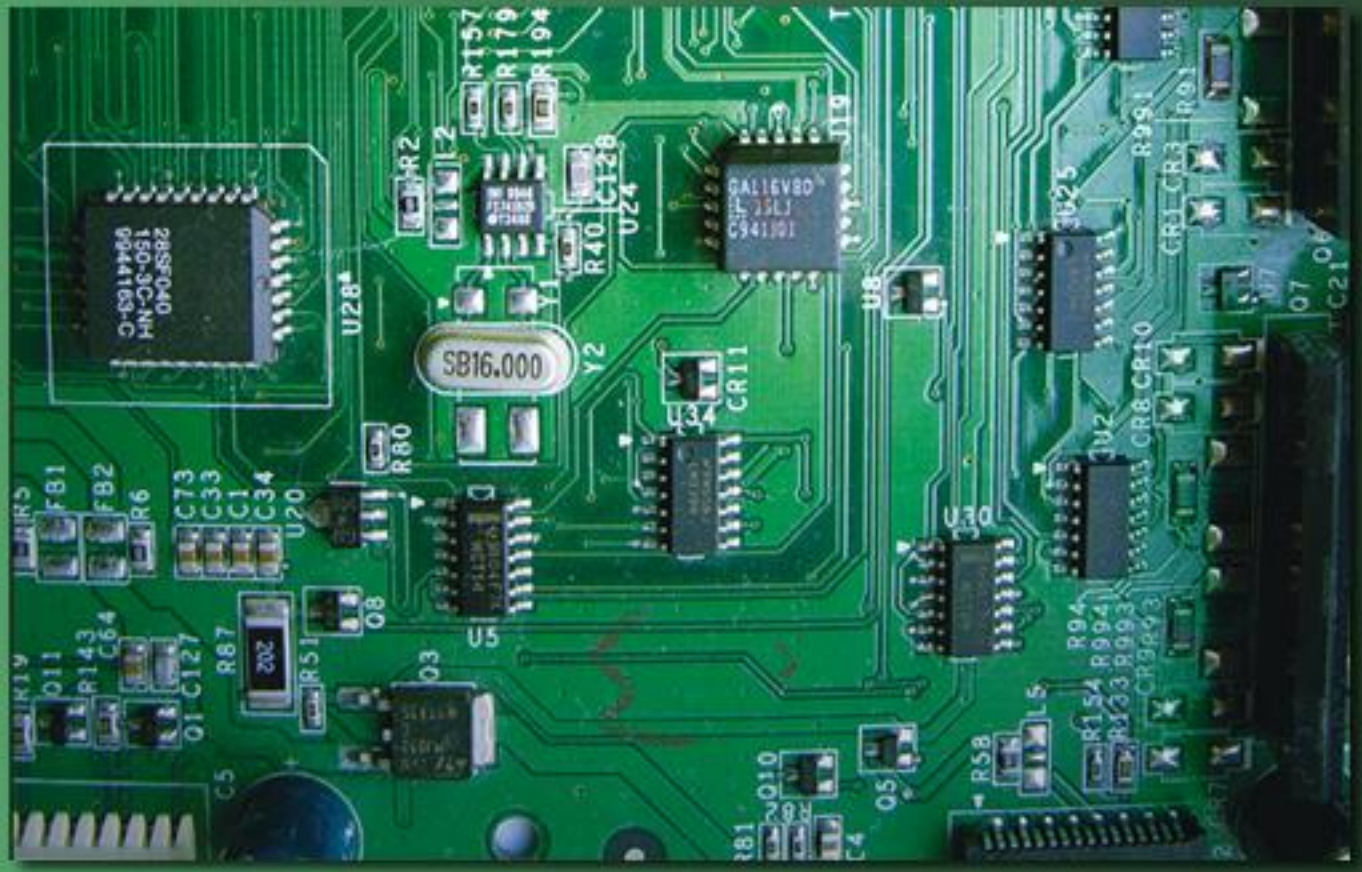
The Intel Microprocessors

8086/8088, 80186/80188, 80286, 80386, 80486 Pentium, Pentium Pro Processor, Pentium II, Pentium 4, and Core2 with 64-bit Extensions

Architecture, Programming, and Interfacing



EIGHTH EDITION

Barry B. Brey

PEARSON

Chapter 10: Memory Interface

Introduction

- Simple or complex, every microprocessor-based system has a memory system.
- Almost all systems contain two main types of memory: **read-only memory** (ROM) and **random access memory** (RAM) or read/write memory.
- This chapter explains how to interface both memory types to the Intel family of microprocessors.

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Chapter Objectives

Upon completion of this chapter, you will be able to:

- Decode the memory address and use the outputs of the decoder to select various memory components.
- Use programmable logic devices (PLDs) to decode memory addresses.
- Explain how to interface both RAM and ROM to a microprocessor.

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10–1 MEMORY DEVICES

- Before attempting to interface memory to the microprocessor, it is essential to understand the operation of memory components.
- In this section, we explain functions of the four common types of memory:
  - read-only memory (ROM)
  - Flash memory (EEPROM)
  - Static random access memory (SRAM)
  - dynamic random access memory (DRAM)

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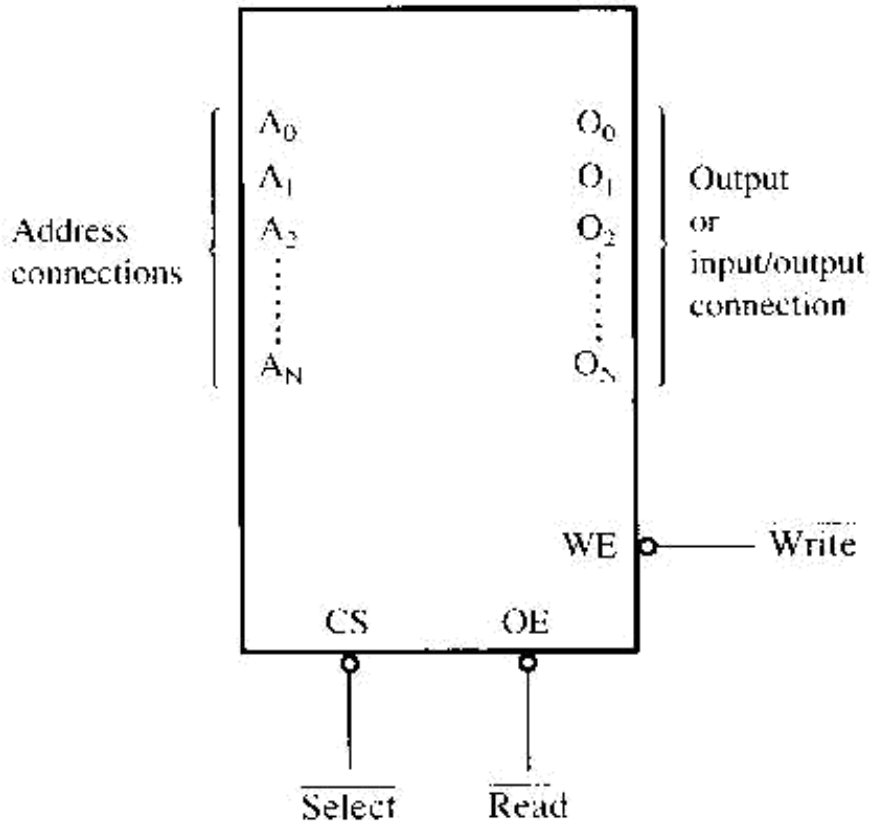
Memory Pin Connections



- address inputs
- data outputs or input/outputs
- some type of selection input
- at least one control input to select a read or write operation

Figure 10–1 A pseudomemory component illustrating the address, data, and control connections.

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Address Connections

- Memory devices have address inputs to select a memory location within the device.
- Almost always labeled from A_0, the least significant address input, to A_n
  - where subscript n can be any value
  - always labeled as one less than total number of address pins
- A memory device with 10 address pins has its address pins labeled from A_0 to A_9.

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- The number of address pins on a memory device is determined by the number of memory locations found within it.
- Today, common memory devices have between 1K (1024) to 1G (1,073,741,824) memory locations.
  - with 4G and larger devices on the horizon
- A 1K memory device has 10 address pins.
  - therefore, 10 address inputs are required to select any of its 1024 memory locations

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- It takes a 10-bit binary number to select any single location on a 1024-location device.
  - 1024 different combinations
  - if a device has 11 address connections, it has 2048 (2K) internal memory locations
- The number of memory locations can be extrapolated from the number of pins.

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Data Connections

- All memory devices have a set of data outputs or input/outputs.
  - today, many devices have bidirectional common I/O pins
  - data connections are points at which data are entered for storage or extracted for reading
- Data pins on memory devices are labeled D_0 through D_7 for an 8-bit-wide memory device.

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- An 8-bit-wide memory device is often called a **byte-wide** memory.
  - most devices are currently 8 bits wide,
  - some are 16 bits, 4 bits, or just 1 bit wide
- Catalog listings of memory devices often refer to memory locations times bits per location.
  - a memory device with 1K memory locations and 8 bits in each location is often listed as a 1K $\times$ 8 by the manufacturer
- Memory devices are often classified according to total bit capacity.

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Selection Connections

- Each memory device has an input that selects or enables the memory device.
  - sometimes more than one
- This type of input is most often called a **chip select** ($\overline{G2A}$) **chip enable** ($\overline{CE}$) or simply **select** ($\overline{S}$) input.
- RAM memory generally has at least one input, and ROM has at least one
- If more than one $\overline{CE}$ connection is present, all must be activated to read or write data.

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Control Connections

- All memory devices have some form of control input or inputs.
  - ROM usually has one control input, while RAM often has one or two control inputs
- Control input often found on ROM is the **output enable** or **gate** connection, which allows data flow from output data pins.
- The $\overline{OE}$ connection enables and disables a set of three-state buffers located in the device and must be active to read data.

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- RAM has either one or two control inputs.
  - if one control input, it is often called R/$\overline{W}$
- If the RAM has two control inputs, they are usually labeled $\overline{WE}$ (or $\overline{W}$), and $\overline{OE}$ (or $\overline{G}$).
  - **write enable** must be active to perform memory write, and $\overline{OE}$ active to perform a memory read
  - when the two controls are present, they must never both be active at the same time
- If both inputs are inactive, data are neither written nor read.
  - the connections are at their high-impedance state

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ROM Memory

- **Read-only memory** (ROM) permanently stores programs/data resident to the system.
  - and must not change when power disconnected
- Often called **nonvolatile memory**, because its contents *do not* change even if power is disconnected.
- A device we call a ROM is purchased in mass quantities from a manufacturer.
  - programmed during fabrication at the factory

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- The EPROM (**erasable programmable read-only memory**) is commonly used when software must be changed often.
  - or when low demand makes ROM uneconomical
  - for ROM to be practical at least 10,000 devices must be sold to recoup factory charges
- An EPROM is programmed in the field on a device called an EPROM programmer.
- Also erasable if exposed to high-intensity ultraviolet light.
  - depending on the type of EPROM

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- PROM memory devices are also available, although they are not as common today.
- The PROM (**programmable read-only memory**) is also programmed in the field by burning open tiny NI-chrome or silicon oxide fuses.
- Once it is programmed, it cannot be erased.

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- A newer type of **read-mostly memory** (RMM) is called the **flash memory**.
  - also often called an EEPROM (**electrically erasable programmable ROM**)
  - EAROM (**electrically alterable ROM**)
  - or a NOVRAM (**nonvolatile RAM**)
- Electrically erasable in the system, but they require more time to erase than normal RAM.
- The flash memory device is used to store setup information for systems such as the video card in the computer.

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- Flash has all but replaced the EPROM in most computer systems for the BIOS.
  - some systems contain a password stored in the flash memory device
- Flash memory has its biggest impact in memory cards for digital cameras and memory in MP3 audio players.
- Figure 10–3 illustrates the 2716 EPROM, which is representative of most common EPROMs.

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- The basic speed of this EPROM is 450 ns.
  - recall that 8086/8088 operated with a 5 MHz clock allowed memory 460 ns to access data
- This type of component requires wait states to operate properly with 8086/8088 because of its rather long access time.
  - if wait states are not desired, higher-speed EPROMs are available at additional cost
  - EPROM memory is available with access times of as little as 100 ns
- Obviously, wait states are required in modern microprocessors for any EPROM device.

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Static RAM (SRAM) Devices

- Static RAM memory devices retain data for as long as DC power is applied.
- Because no special action is required to retain data, these devices are called **static memory**.
  - also called **volatile memory** because they will not retain data without power
- The main difference between ROM and RAM is that RAM is written under normal operation, whereas ROM is programmed outside the computer and normally is only read.

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- Fig 10–4 illustrates the 4016 SRAM,
  - a 2K × 8 read/write memory
- This device is representative of all SRAM devices.
  - except for the number of address and data connections.
- The control inputs of this RAM are slightly different from those presented earlier.
  - however the control pins function exactly the same as those outlined previously
- Found under part numbers 2016 and 6116.

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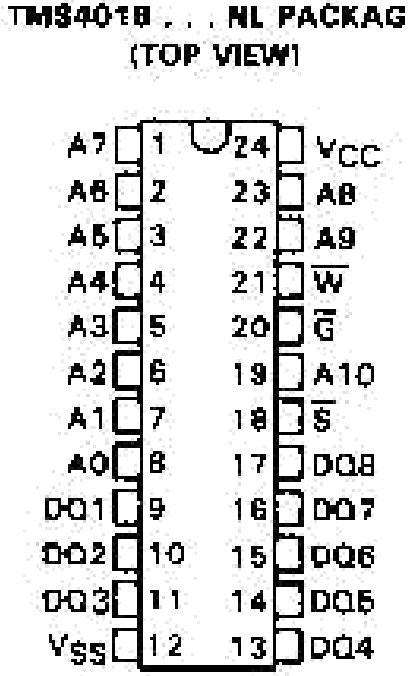
Figure 10–4 The pin-out of the TMS4016, 2K × 8 static RAM (SRAM). (Courtesy of Texas Instruments Incorporated.)



PIN NOMENCLATURE	
A0 – A10	Addresses
DQ1 – DQ8	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{S}$	Chip Select
V_{CC}	+5 V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

- One important piece of information provided by the timing diagram and data sheet is the memory access time
- that is the time it takes the memory to read information

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- Figure 10–6 illustrates pin-outs of the 62256, 32K × 8 static RAM.
- Packaged in a 28-pin integrated circuit
- Available with access times of 120 or 150 ns.
- Other common SRAM devices are
  - 8K × 8; 128K × 8; 256K × 8
  - 512K × 8; 1M × 8
- Access times can be as low as 1.0 ns for SRAM used in computer cache memory.

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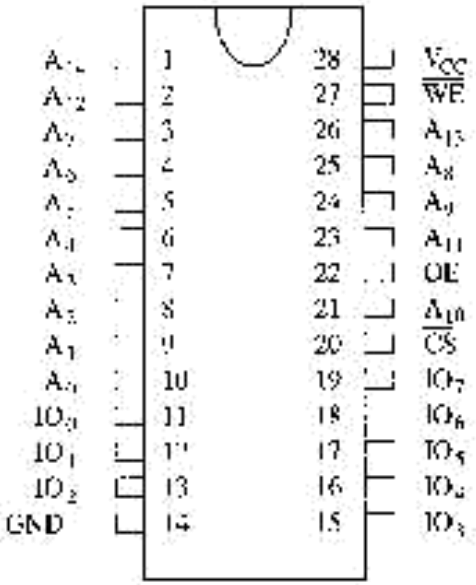
Figure 10–6 The pin-out of the TMS62256, 32K × 8 static RAM (SRAM). (Courtesy of Texas Instruments Incorporated.)



- SRAM is used when the size of the read/write memory is relatively small
- today, a small memory is less than 1M byte

PIN FUNCTION

A_0 - A_{14}	Addresses
IO_0 - IO_7	Data connections
CS	Chip select
OE	Output enable
WE	Write enable
V_{CC}	+5V Supply
GND	Ground

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Dynamic RAM (DRAM) Memory

- Available up to 256M × 8 (2G bits).
- DRAM is essentially the same as SRAM, except that it retains data for only 2 or 4 ms on an integrated capacitor.
- After 2 or 4 ms, the contents of the DRAM must be completely rewritten *(refreshed)*.
  - because the capacitors, which store a logic 1 or logic 0, lose their charges

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- In DRAM, the entire contents are refreshed with 256 reads in a 2- or 4-ms interval.
  - also occurs during a write, a read, or during a special refresh cycle
- DRAM requires so many address pins that manufacturers multiplexed address inputs.
- Figure 10–7 illustrates a 64K $\times$ 4 DRAM, the TMS4464, which stores 256K bits of data.
  - note it contains only eight address inputs where it should contain 16—the number required to address 64K memory locations

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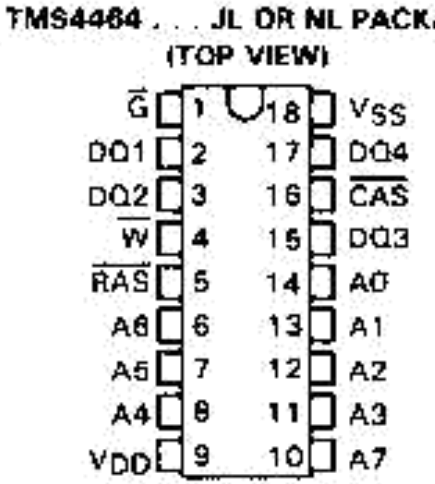
Figure 10–7 The pin-out of the TMS4464, 64K × 4 dynamic RAM (DRAM). (Courtesy of Texas Instruments Incorporated.)



(a)

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ1-DQ4	Data-In/Data-Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

(b)

- the access time is $t_{a(A)}$
- on the slowest 4016, this time is 250 ns, fast enough to connect directly to an 8088/8086 at 5 MHz, without wait states
- access time must always be checked to determine compatibility of memory components

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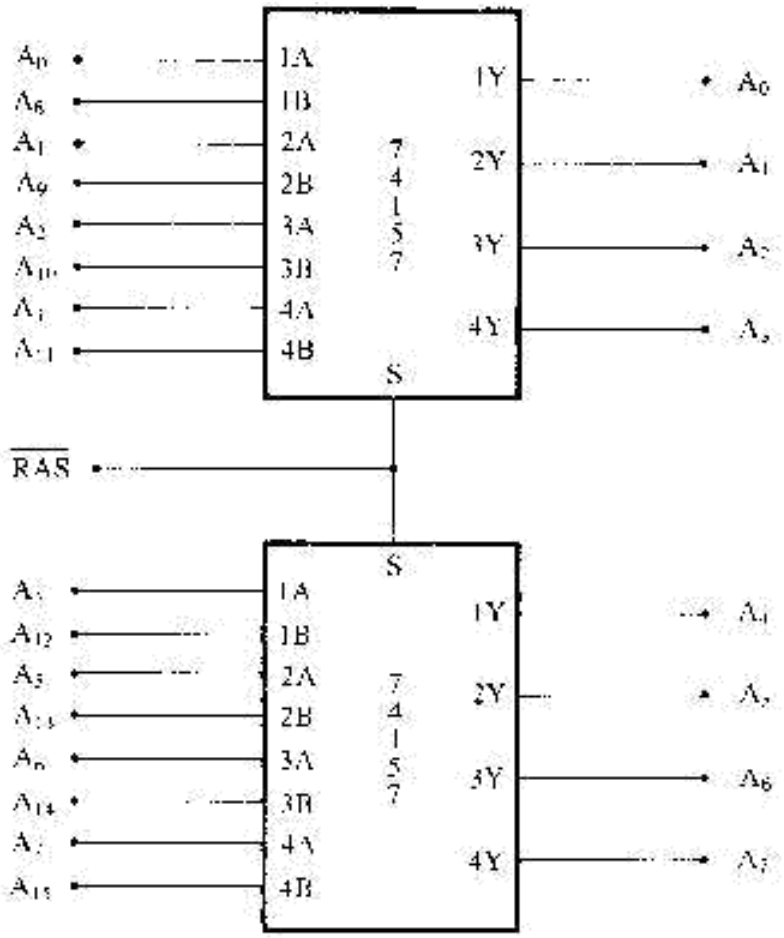
Figure 10–9 Address multiplexer for the TMS4464 DRAM.



- 16 address bits can be forced into eight address pins in two 8-bit increments
- this requires two special pins: the **column address strobe** ($\overline{\text{CAS}}$) and **row address strobe** ($\overline{\text{RAS}}$)

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- First, A_0–A_7 are placed on the address pins and strobed into an internal row latch by $\overline{RAS}$ as the row address.
- Next, address bits A_8-A_{15} are placed on the same eight address inputs and strobed into an internal column latch by $\overline{CAS}$ as the column address
- The 16-bit address in the internal latches addresses the contents of one of the 4-bit memory locations.
  - $\overline{CAS}$ also performs chip selection input to DRAM

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- Figure 10-10 shows the pin-out of the 41256 dynamic RAM
- this device is organized as a 256K $\times$ 1 memory
- requires as little as 70 ns to access data

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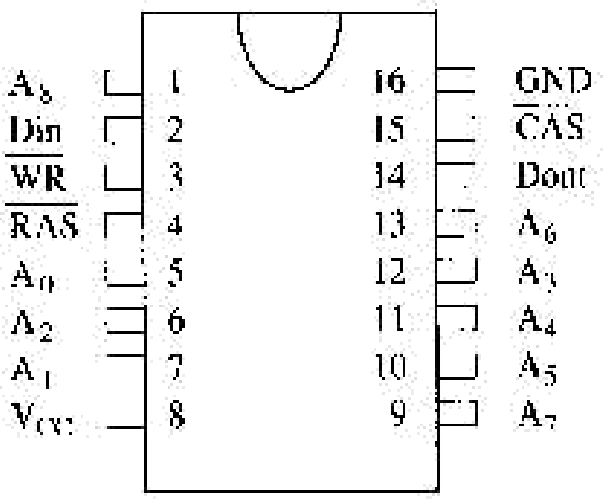
Figure 10–10 The 41256 dynamic RAM organized as a 256K × 1 memory device.



PIN FUNCTIONS

A_0 A_8	Addresses
Din	Data in
Dout	Data out
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{WR}$	Write enable
V_{CC}	+5V Supply
GND	Ground

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- DRAM is often placed on small boards called SIMMs (Single In-Line Memory Modules).
- The 30-pin SIMM is organized most often as 1M × 8 or 1M × 9, and 4M × 8 or 4M × 9.
  - illustrated in Fig 10–11 is a 4M × 9
  - the ninth bit is the parity bit
- Also shown is a newer 72 pin SIMM.
- 72-pin SIMMs are often organized as 1M × 32 or 1M × 36 (with parity).
- Fig 10–11 illustrates a 4M × 36 SIMM, which has 16M bytes of memory

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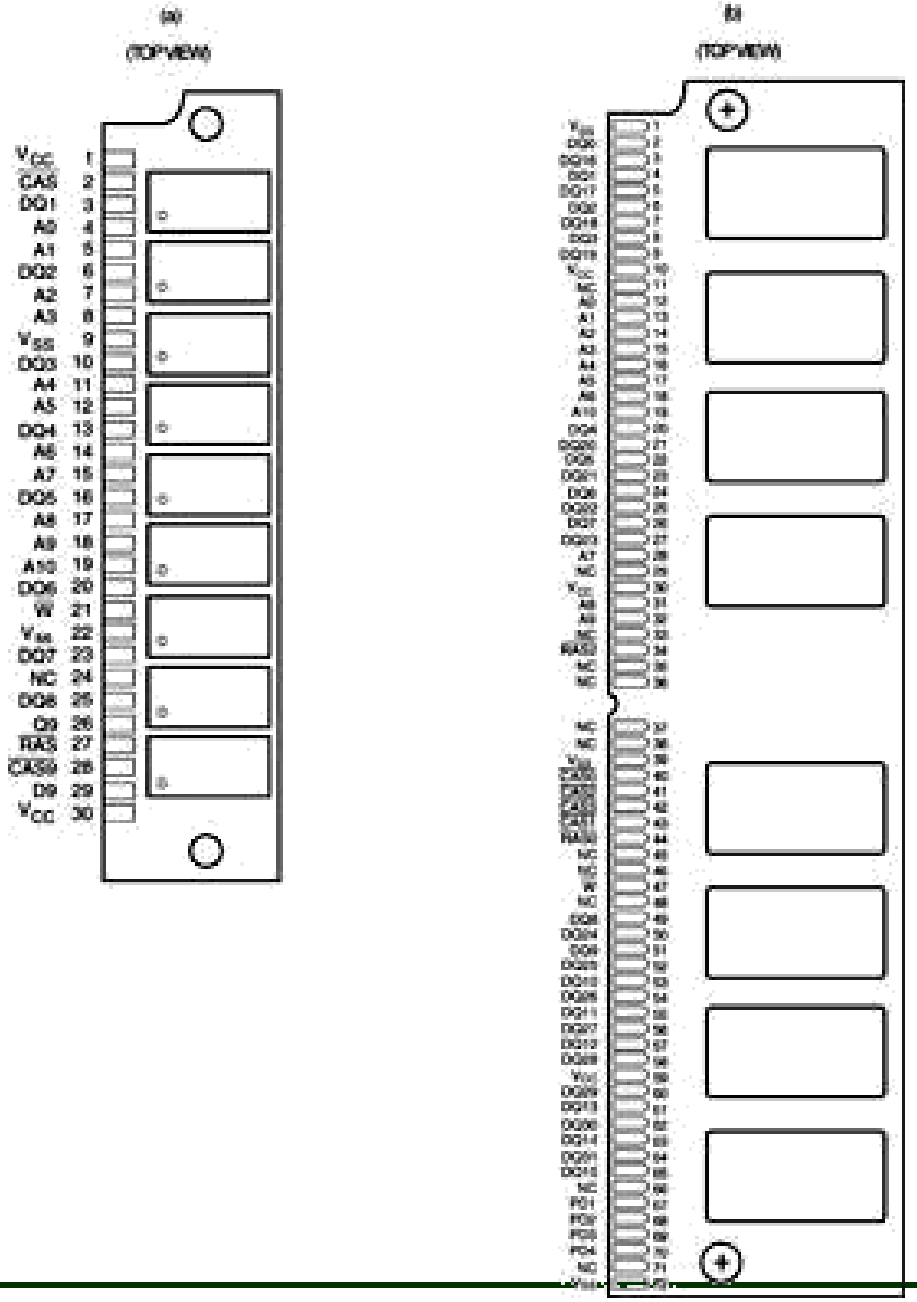

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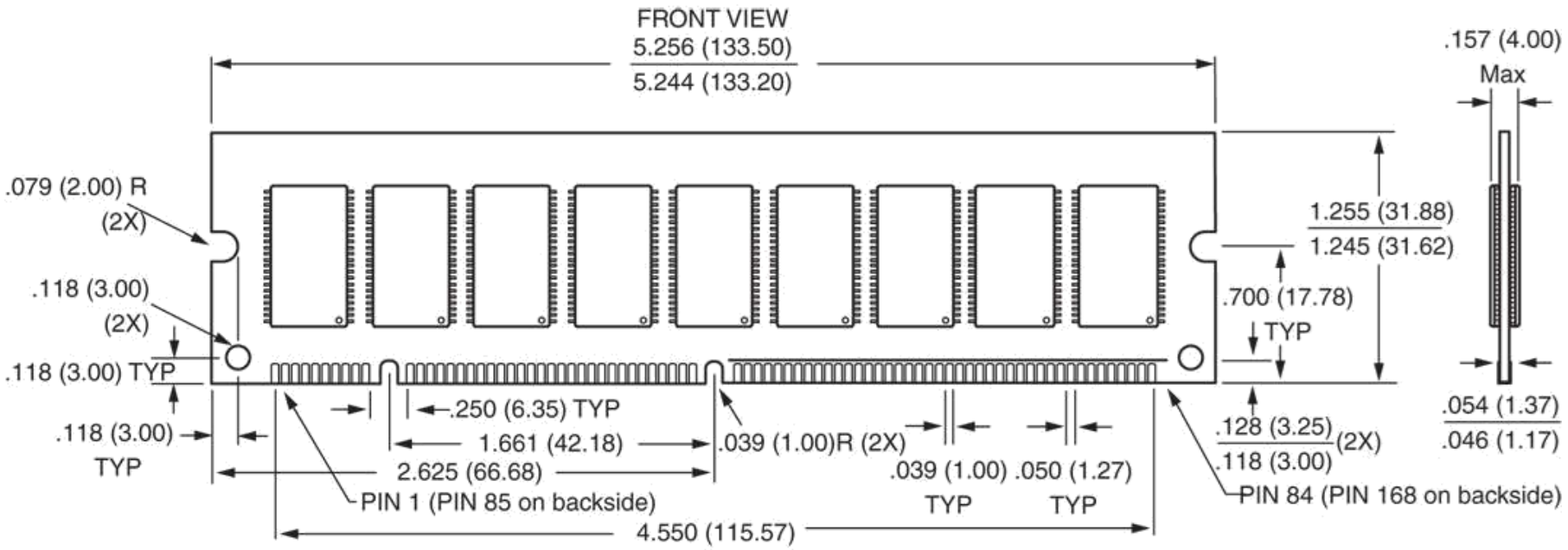

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- Pentium–Pentium 4 microprocessors have a 64-bit wide data bus, which precludes use of the 8-bit-wide SIMMs described here.
  - 72-pin SIMMs are cumbersome as they must be paired to obtain a 64-bit-wide data connection
- 64-bit-wide DIMMs (Dual In-line Memory Modules) have become the standard.
- The memory on these modules is organized as 64 bits wide.
- Common sizes available are from 16M bytes (2M $\times$ 64) to 1G bytes (128M $\times$ 64).

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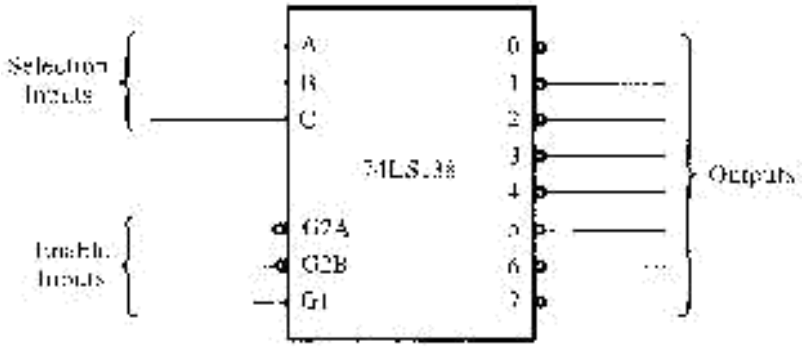
Figure 10–12 The pin-out of a 168-pin DIMM.



Inputs						Outputs							
Enable			Select										
G2A	G2B	G1	C	B	A	0	1	2	3	4	5	6	7
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

- The DIMM module is available in DRAM, EDO, SDRAM, and DDR (double-data rate) forms, with or without an EPROM.
- The EPROM provides information to the system on the size and the speed of the memory device for plug-and-play applications.

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- Another type is the RIMM memory module from RAMBUS Corporation,
  - this memory type has faded from the market
- The latest DRAM is the DDR (**double-data rate**) memory device and DDR2.
  - DDR transfers data at each edge of the clock, making it operate at twice the speed of SDRAM
- Many wait states are still required to operate this type of memory, but it can be much faster than normal SDRAM memory, including RDRAM.

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10–2 ADDRESS DECODING

- In order to attach a memory device to the microprocessor, it is necessary to decode the address sent from the microprocessor.
- Decoding makes the memory function at a unique section or partition of the memory map.
- Without an address decoder, only one memory device can be connected to a microprocessor, which would make it virtually useless.

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Why Decode Memory?

- The 8088 has 20 address connections and the 2716 EPROM has 11 connections.
- The 8088 sends out a 20-bit memory address whenever it reads or writes data.
  - because the 2716 has only 11 address pins, there is a mismatch that must be corrected
- The decoder corrects the mismatch by decoding address pins that do not connect to the memory component.

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Simple NAND Gate Decoder

- When the 2K × 8 EPROM is used, address connections A_{10}–A_0 of 8088 are connected to address inputs A_{10}–A_0 of the EPROM.
  - the remaining nine address pins (A_{19}–A_{11}) are connected to a NAND gate decoder
- The decoder selects the EPROM from one of the 2K-byte sections of the 1M-byte memory system in the 8088 microprocessor.
- In this circuit a NAND gate decodes the memory address, as seen in Figure 10-13.

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Figure 10–13 A simple NAND gate decoder that selects a 2716 EPROM for memory location FF800H–FFFFFH.

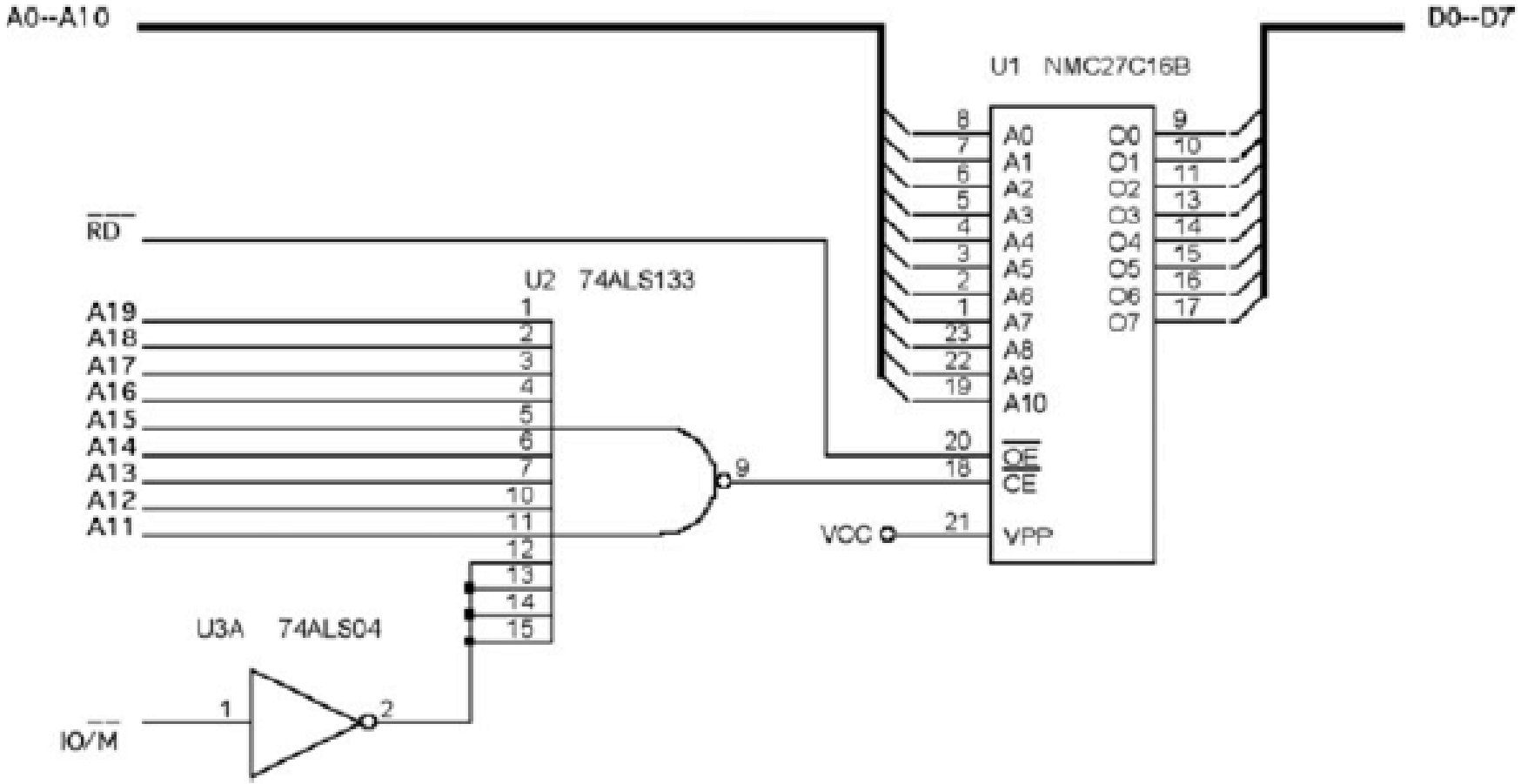

FIGURE 10–13 A simple NAND gate decoder that selects a 2716 EPROM for memory location FF800H–FFFFFH.

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- If the 20-bit binary address, decoded by the NAND gate, is written so that the leftmost nine bits are 1s and the rightmost 11 bits are don't cares (X), the actual address range of the EPROM can be determined.
  - a *don't care* is a logic 1 or a logic 0, whichever is appropriate
- Because of the excessive cost of the NAND gate decoder and inverters often required, this option requires an alternate way.

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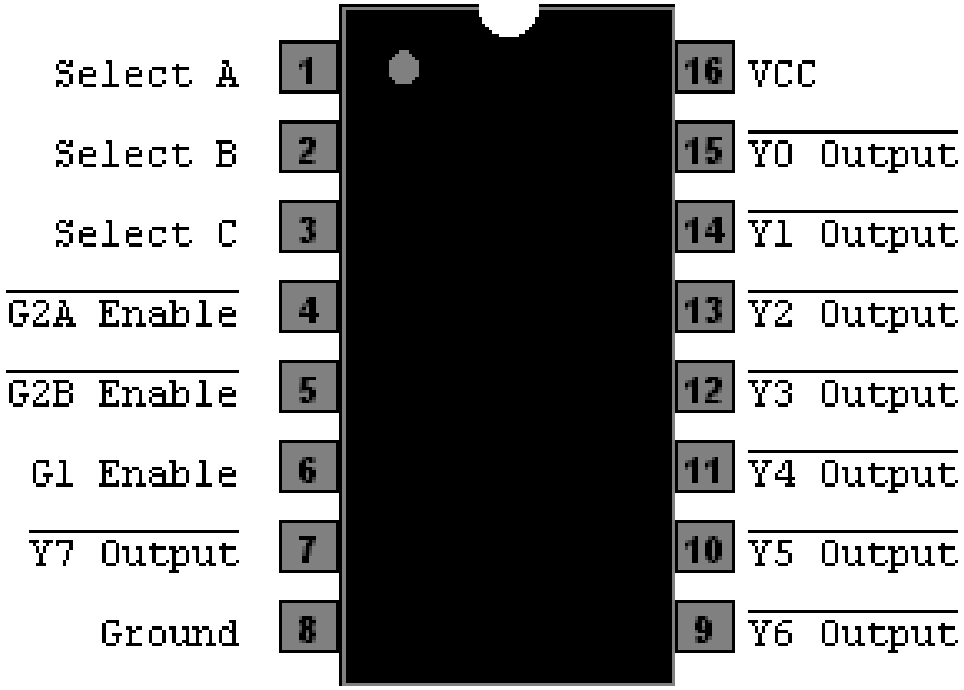
The 3-to-8 Line Decoder (74LS138)

A common integrated circuit decoder found in many systems is the 74LS138 3-to-8 line decoder.



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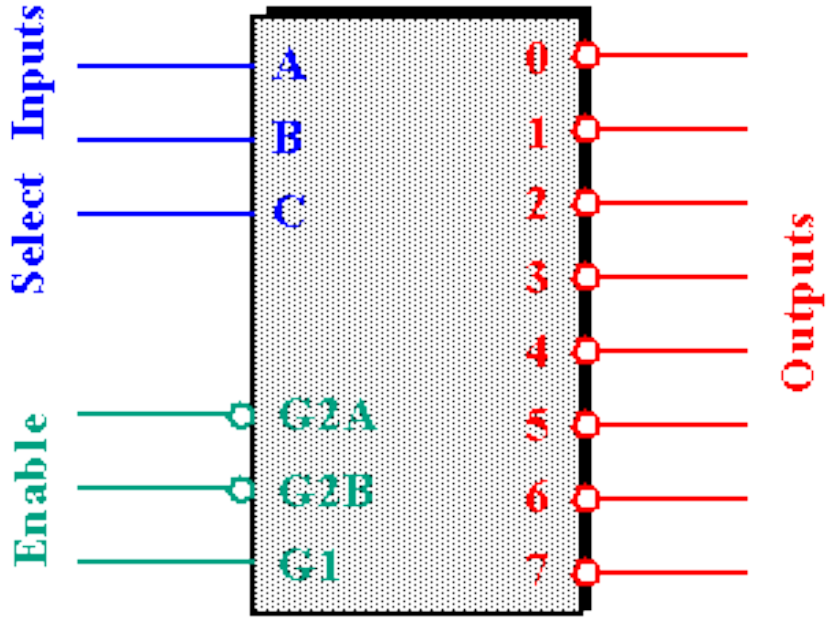
The 3-to-8 Line Decoder (74LS138)



Inputs						Output							
Enable			Select										
G2A	G2B	G1	C	B	A	0	1	2	3	4	5	6	7
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

Figure 10–14 The 74LS138 3-to-8 line decoder and function table.

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Sample Decoder Circuit

- The outputs of the decoder in Figure 10–15, are connected to eight different 2764 EPROM memory devices.
- The decoder selects eight 8K-byte blocks of memory for a total capacity of 64K bytes.
- This figure also illustrates the address range of each memory device and the common connections to the memory devices.

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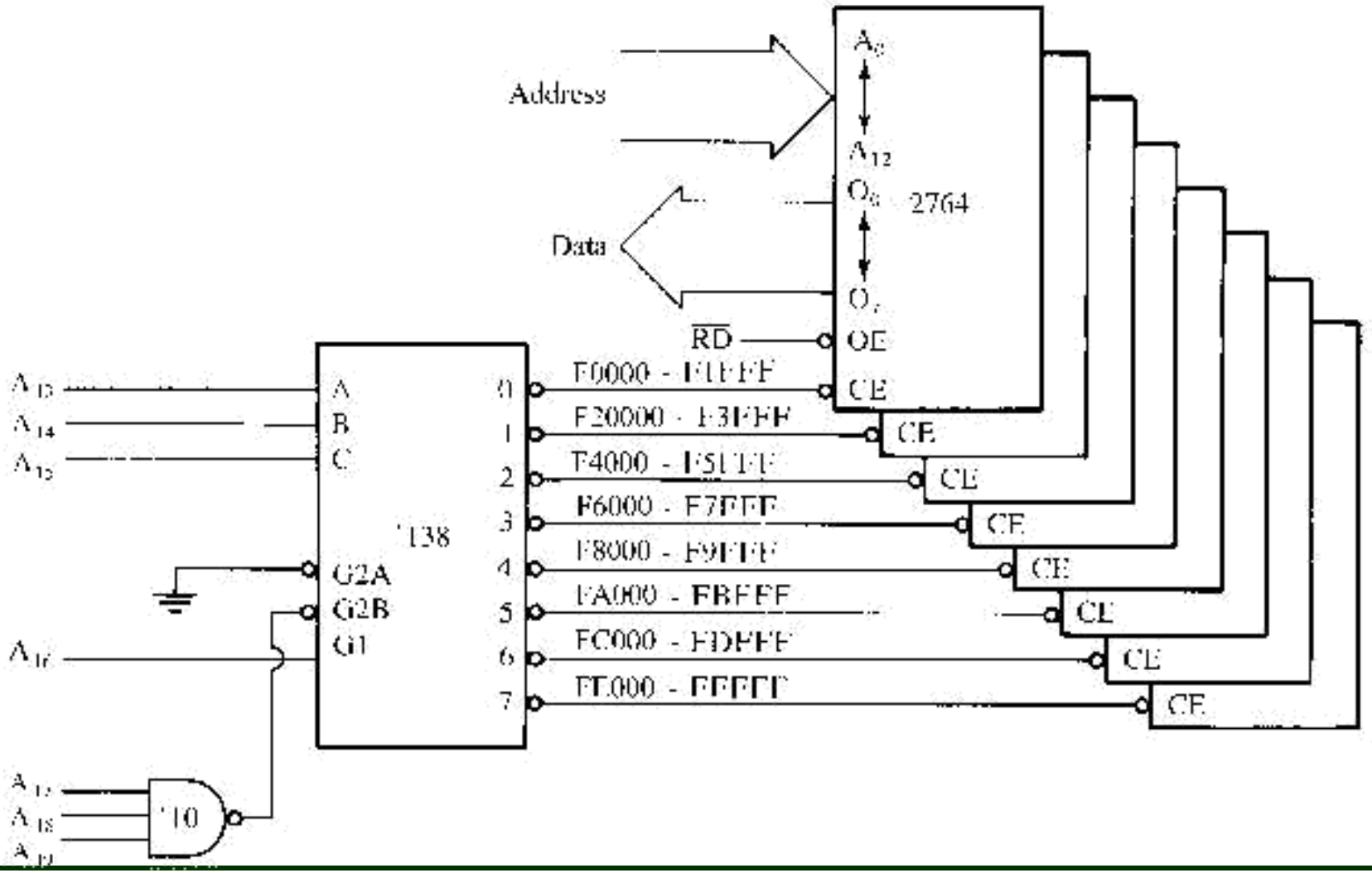
Figure 10–15 A circuit that uses eight 2764 EPROMs for a 64K × 8 section of memory in an 8088 microprocessor-based system. The addresses selected in this circuit are F0000H–FFFFFH.



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- In this circuit, a three-input NAND gate is connected to address bits A_{19}–A_{17}.
- When all three address inputs are high, the output of this NAND gate goes low and enables input $\overline{G2B}$ of the 74LS138.
- Input G1 is connected directly to A_{16}.
- In order to enable this decoder, the first four address connections (A_{19}–A_{16}) must all be high.

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- Address inputs C, B, and A connect to microprocessor address pins A_{15}–A_{13}.
- These three address inputs determine which output pin goes low and which EPROM is selected whenever 8088 outputs a memory address within this range to the memory system.

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The Dual 2-to-4 Line Decoder (74LS139)

- Figure 10–16 illustrates both the pin-out and the truth table for the 74LS139 dual 2-to-4 line decoder.
- 74LS139 contains two separate 2-to-4 line decoders—each with its own address, enable, and output connections.
- A more complicated decoder using the 74LS139 decoder appears in Figure 10–17.

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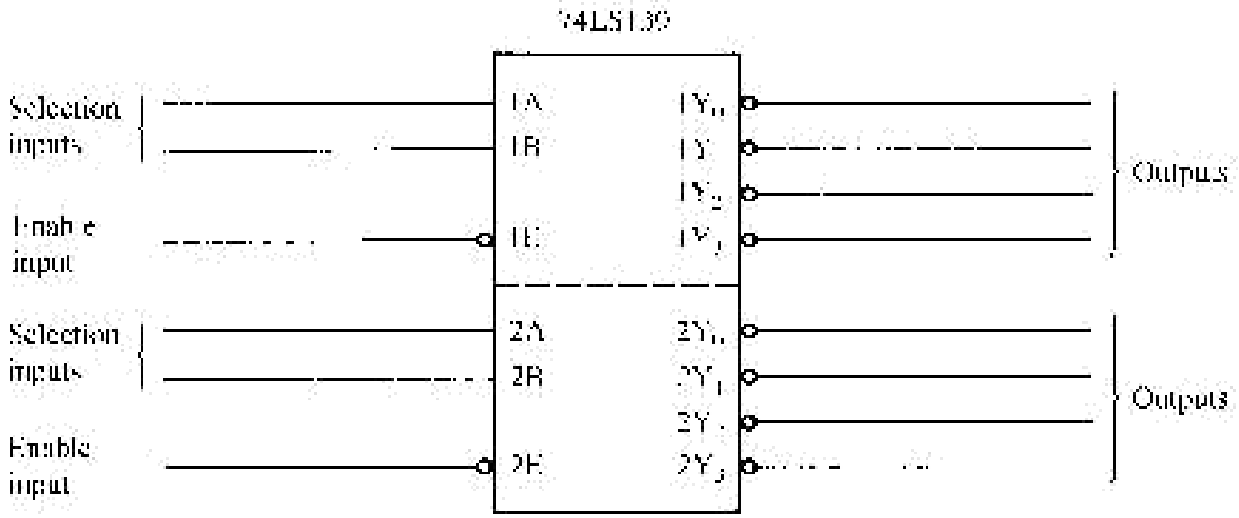
Figure 10–17 A sample memory system constructed with a 74HCT139.



Inputs			Outputs			
$\overline{E}$	A	B	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	X	X	1	1	1	1

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10–3 8088 and 80188 (8-bit) MEMORY INTERFACE

- In this section, we examine the memory interface to both RAM and ROM and explain the error-correction code (ECC), which is still is currently available to memory system designers.
- Many home computer systems do not use ECC because of the cost, but business machines often do use it.

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Basic 8088/80188 Memory Interface

- 8088/80188 microprocessors have an 8-bit data bus, which makes them ideal to connect to common 8-bit memory devices available.
- For the 8088/80188 to function correctly with memory, however, the system must decode the address to select a memory component.

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Interfacing EPROM to the 8088

- Fig 10–20 shows an 8088/80188 connected to three 27256 EPROMs, 32K × 8 devices.
  - 74HCT138 decoder in this illustration decodes three 32K × 8 blocks of memory for a total of 96K × 8 bits of physical address space for 8088/80188
- The decoder is selected for an address range that begins at E8000H and continues through location FFFFFH—the upper 96K bytes of memory.

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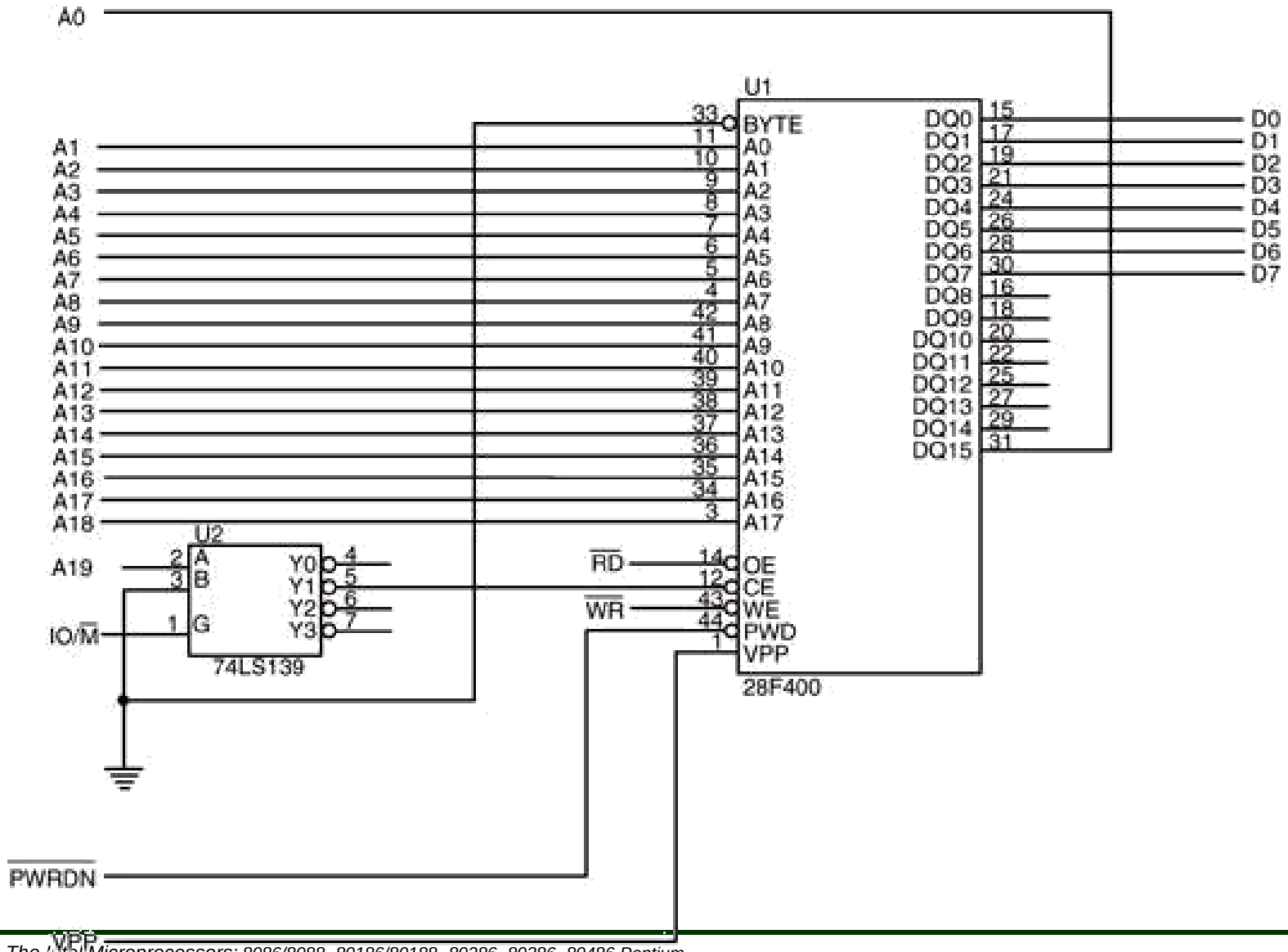
Figure 10–20 Three 27256 EPROMs interfaced to the 8088 microprocessor.



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- This section of memory is an EPROM because FFFF0H is where the 8088 starts to execute instructions after a hardware reset.
  - often called the **cold-start location**
- The software stored in this section of memory would contain a JMP instruction at location FFFF0H that jumps to location E8000H
  - so the remainder of the program can execute
- In this circuit, U_1 is decoded at addresses E8000H–EFFFFH, U_2 is decoded at F0000H–F7FFFH, and U_3 at F8000H–FFFFFH.

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Interfacing RAM to the 8088

- RAM is easier to interface than EPROM as most RAM does not require wait states.
  - ideal section of memory for RAM is the very bottom, which contains vectors for interrupts
- Interrupt vectors are often modified by software packages,
  - it important to encode this section of the memory with RAM
- Fig 10–21 shows sixteen 62256 static RAMs interfaced to the 8088, beginning at 00000H.

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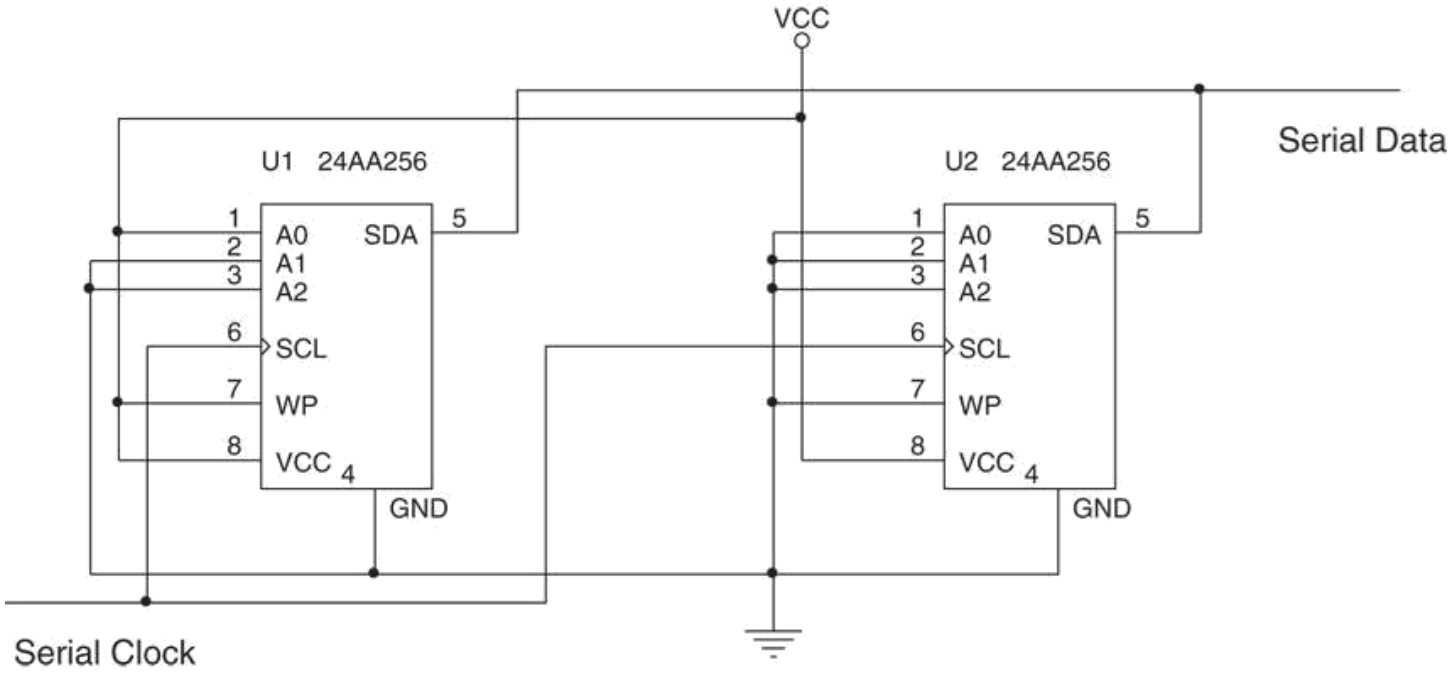
Figure 10–21 A 512K-byte static memory system using 16 62255 SRAMs.



- this board uses two decoders to select 16 RAM components, and a third to select other decoders for the appropriate memory sections
- sixteen 32K RAMs fill memory from 00000H through 7FFFFH, for 512K bytes memory.

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Interfacing Flash Memory

- Becoming commonplace for storing setup information on video cards, and the system BIOS in the personal computer.
  - also in MP3 players and USB pen drives
- Flash memory is also found in many other applications to store information that is only changed occasionally.

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- The difference between flash memory and SRAM is that flash requires 12V programming voltage to erase and write new data.
- The newest versions of flash memory are erased with a 5.0V or even a 3.3V signal
  - so a converter is not needed
- EEPROM is available as a memory device with a parallel or serial interface.
- Serial is too small for memory expansion, but as an I/O it can store information.
  - such as in a flash drive.

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- Fig 10–22 shows a 28F400 flash memory interfaced to an 8088 parallel interface.
  - 28F400 can be used as a 512K $\times$ 8 memory device or as a 256K $\times$ 16 memory device
  - because it is interfaced to an 8088, the configuration is 512K $\times$ 8
- Control connections on this device are identical to that of an SRAM.
- New pins are for erase and programming; selecting power-down mode when a logic 0; and selecting byte or word operation.

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Figure 10–22 The 28F400 flash memory device interfaced to the 8088 microprocessor.

Write Address

S	1	0	1	0	A2	A1	A0	0	ACK	x	A14	A13	A12	A11	A10	A9	A8	ACK	A7	A6	A5	A4	A3	A2	A1	A0	ACK

Followed by for a Read Byte

S	1	0	1	0	A2	A1	A0	1	ACK	D7	D6	D5	D4	D3	D2	D1	D0	ACK	P

or Followed by for a Write Byte

D7	D6	D5	D4	D3	D2	D1	D0	ACK	P

S = Start
P = Stop
ACK = acknowledge

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SUMMARY

- All memory devices have address inputs; data inputs and outputs, or just outputs; a pin for selection; and one or more pins that control the operation of the memory.
- Address connections on a memory component are used to select one of the memory locations within the device.
- Ten address pins have 1024 combinations and therefore are able to address 1024 different memory locations.

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SUMMARY (*cont.*)

- Data connections on a memory are used to enter information to be stored in a memory location and also to retrieve information read from a memory location.
- Manufacturers list their memory as, for example, 4K x 4, which means that the device has 4K memory locations (4096) and that four bits are stored in each location.

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SUMMARY (*cont.*)

- An EPROM memory is programmed by an EPROM programmer and can be erased if exposed to ultraviolet light.
- Today, EPROMs are available in sizes from 1K x 8 up to 512K x 8 and larger.
- The flash memory (EEPROM) is programmed in the system by using a 12 V or 5.0 V programming pulse.

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SUMMARY (*cont.*)

- Static RAM (SRAM) retains data for as long as the system power supply is attached.
- These memory types are available in sizes up to 128K x 8.

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SUMMARY (*cont.*)

- Dynamic RAM (DRAM) retains data for only a short period, usually 2-4 ms.
- This creates problems for the memory system designer because the DRAM must be refreshed periodically.
- DRAMs also have multiplexed address inputs that require an external multiplexer to provide each half of the address at the appropriate time.

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SUMMARY (*cont.*)

- Memory address decoders select an EPROM or RAM at a particular area of the memory.
- Commonly found address decoders include the 74LS138 3-to-8 line decoder, the 74LS139 2-to-4 line decoder, and programmed selection logic in a PLD.

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SUMMARY (*cont.*)

- The access speed of the EPROM must be compatible with the microprocessor to which it is interfaced.
- Many EPROMs available today have an access time of 450 ns, which is too slow for the 5 MHz 8088.
- In order to circumvent this problem, a wait state is inserted to increase memory access time to 660 ns.

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SUMMARY (*cont.*)

- Error-correction features are also available for memory systems, but these require the storage of many more bits.
- If an 8-bit number is stored with an error-correction circuit, it actually takes 13 bits of memory: five for an error checking code and eight for the data.
- Most error-correction integrated circuits are able to correct only a single-bit error.

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SUMMARY

- Dynamic RAM controllers are designed to control DRAM memory components.
- Many DRAM controllers today are built into the chip set and contain address multiplexers, refresh counters, and the circuitry required to do a periodic DRAM memory refresh.

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